3D Stacked Technologies applied to Custom CMOS Image Sensors

A very solid reason to invest in differentiation

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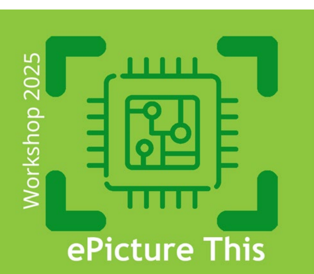


Organized by projects: 2021004 Imagination (Penta)
2023022 Elevation (Xecs)
2024001 Entertain (Xecs)

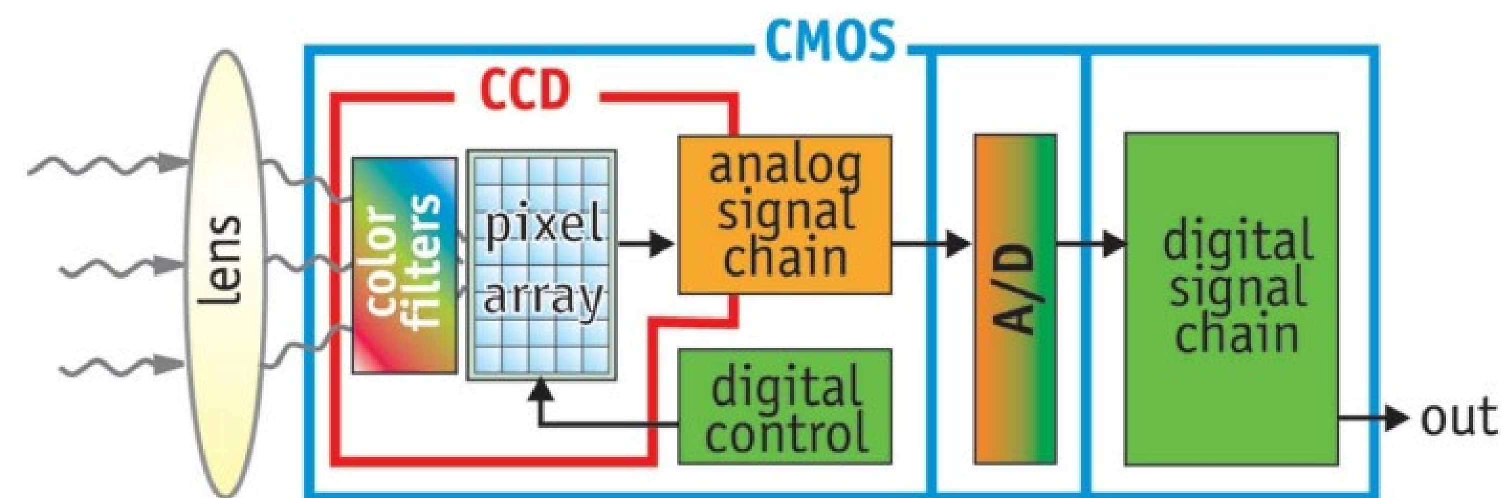
3D stacked technology for CMOS image sensors

CMOS image sensors evolution

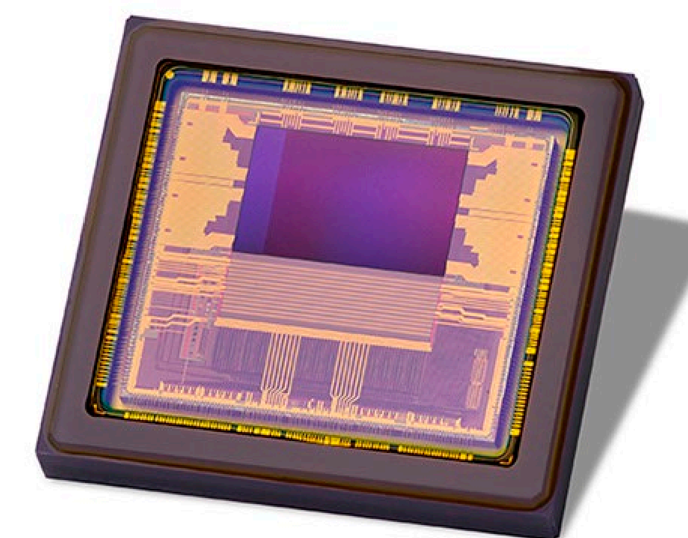
- CMOS technology has been replacing CCD in most applications during the last 20 years

- CMOS technology has enabled reducing the complexity of the cameras by bringing to the sensor:
  - Timing generation
  - Power biasing
  - ADC and control

- More and more functionality has been incorporated to CMOS sensors, up to the point that the pixel array is not the dominant fraction of the die size



Source: Teledyne Dalsa



3D stacked technology for CMOS image sensors

CMOS image sensors evolution

Performance

FSI

BSI

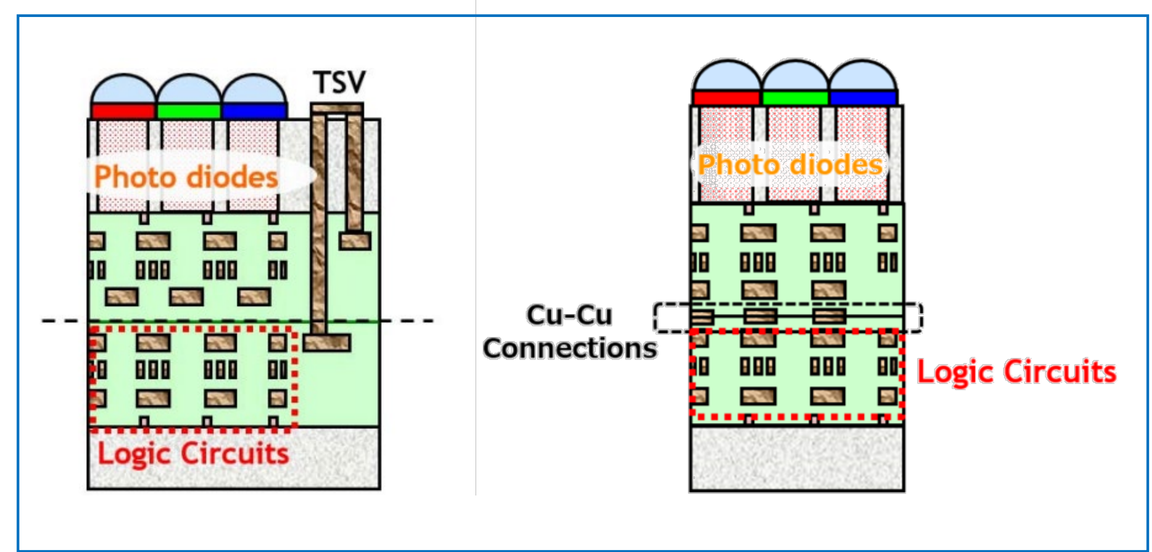
BSI stacked TSV

BSI stacked Hybrid Bonding

BSI multi-stacked TSV + Hybrid

Complexity

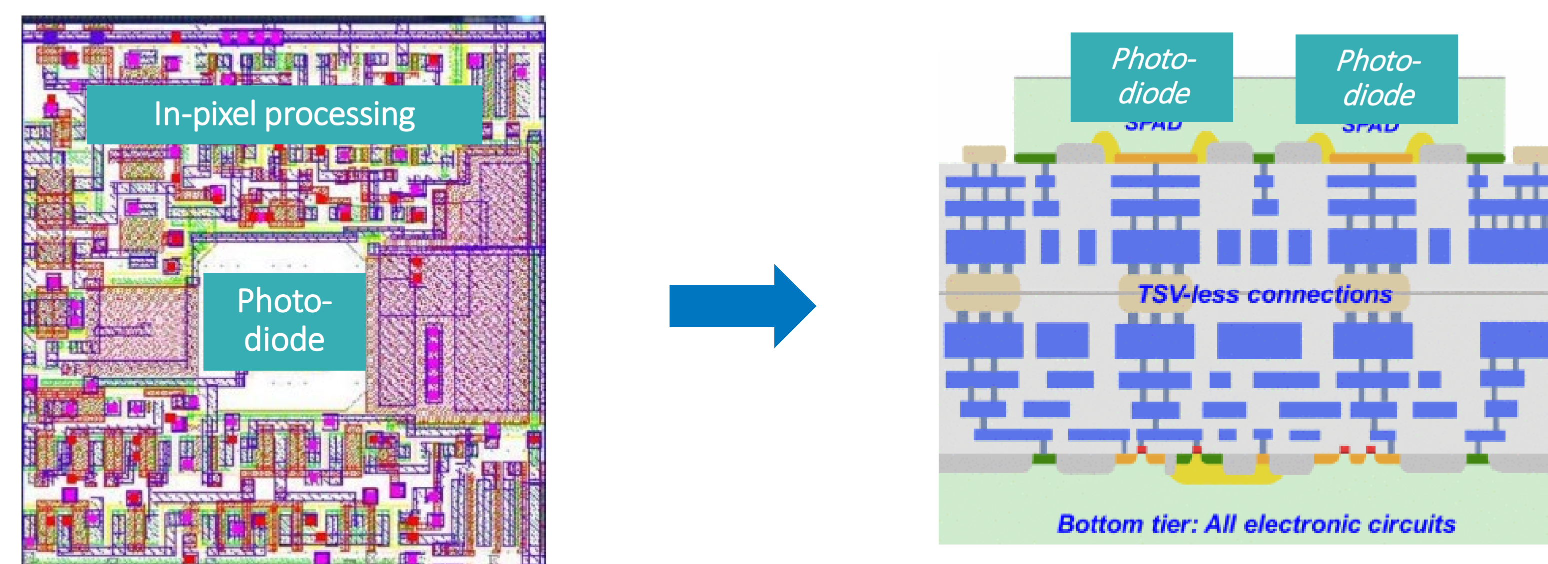
- 3D stacked sensors are an opportunity to bring more and more functionality into the CMOS image sensors in a cost-effective manner
- 3D stacked technology consists of vertically interconnecting the dice coming from different wafers



3D stacked technology for CMOS image sensors

What opportunities, performances, & functionalities are enabled by 3D stacking?

1. Increases fill factor (responsivity) for those pixels with in-pixel extra circuitry

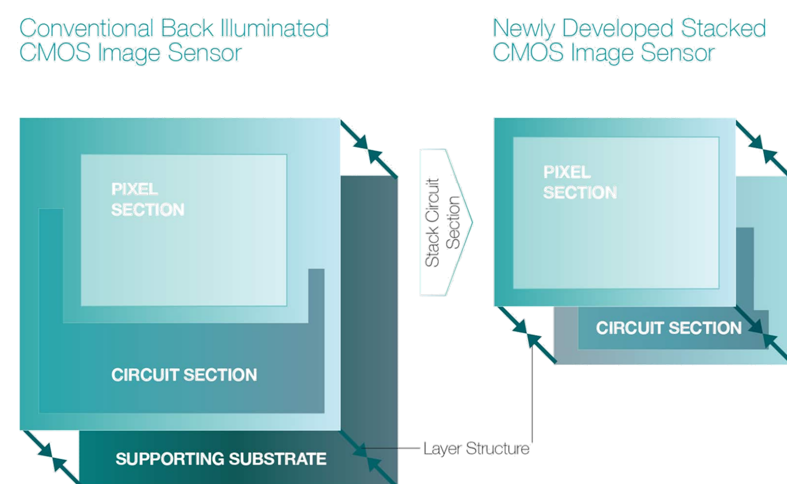


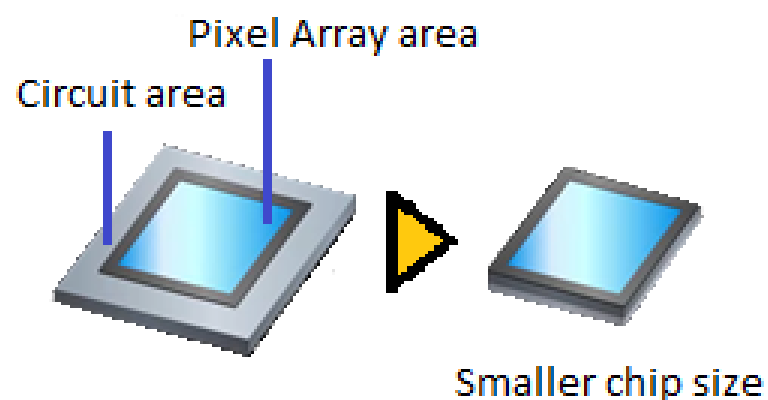
Features	Benefits	Applications
• Enable pixels with multiple memory nodes	• New HDR techniques, more efficient • Reduces artefacts due to motion	• HDR applications • 3D applications (ToF)
• In-pixel connection and circuitry	• Embeds intelligence on-chip targeting multiple functions, from noise reduction to complete image-processing algorithms	• Event-driven vision sensor • Scientific applications (low-noise)

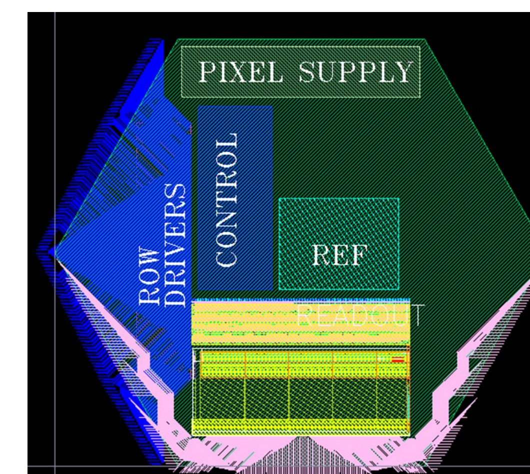
3D stacked technology for CMOS image sensors

What opportunities, performances, & functionalities are enabled by 3D stacking?

2. Removes periphery circuits, reducing the die size



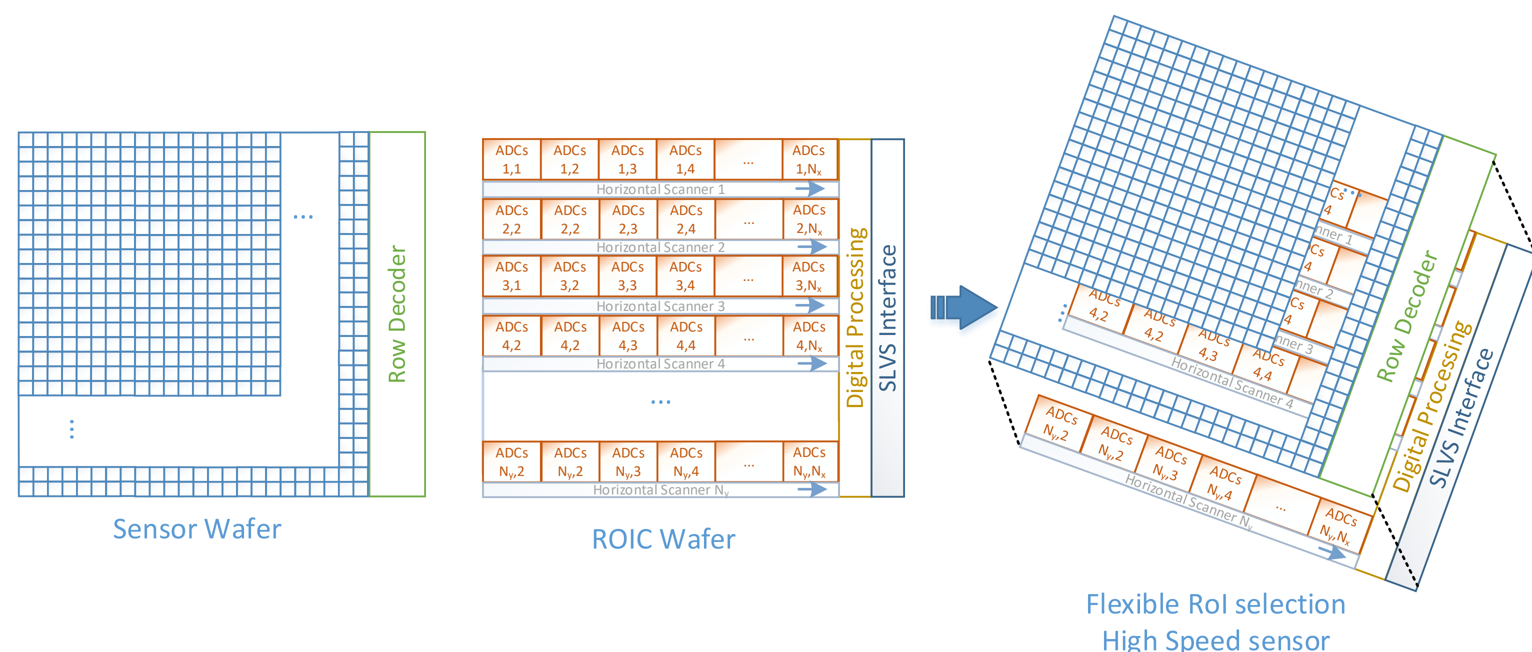




Features	Benefits	Applications
• Reducing die size	• Reducing total size of the system • Cost savings in high volume	• High-volume applications • Endoscopy • Camera miniaturization
• Reducing periphery area	• Butted sensors	• X-Ray applications
• Non-rectangular shapes	• Hexagonal/Octagonal devices, enabling large curved sensing surfaces	• AR, VR

3D stacked technology for CMOS image sensors

What opportunities, performances, & functionalities are enabled by 3D stacking?

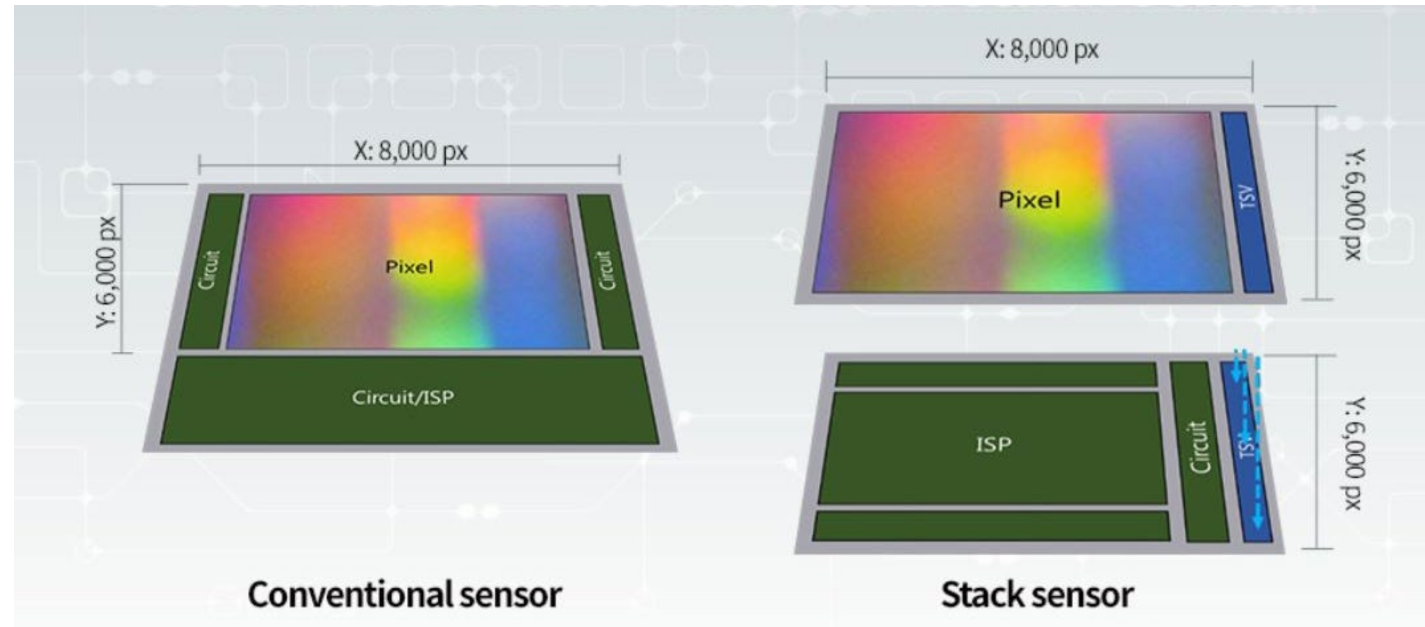


3. Increases parallelism

Features	Benefits	Applications
• Multi-tap readout	• Mitigation of bottleneck introduced by column-parallel ADCs	• High-speed image sensors
• Multi sampling readout	• Noise reduction	• Scientific and low-noise sensors
• Redundant circuitry	• Yield improvement • Improved resilience	• Space sensors
• Cluster control array	• Multi-exposure device	• HDR applications

3D stacked technology for CMOS image sensors

What opportunities, performances, & functionalities are enabled by 3D stacking?



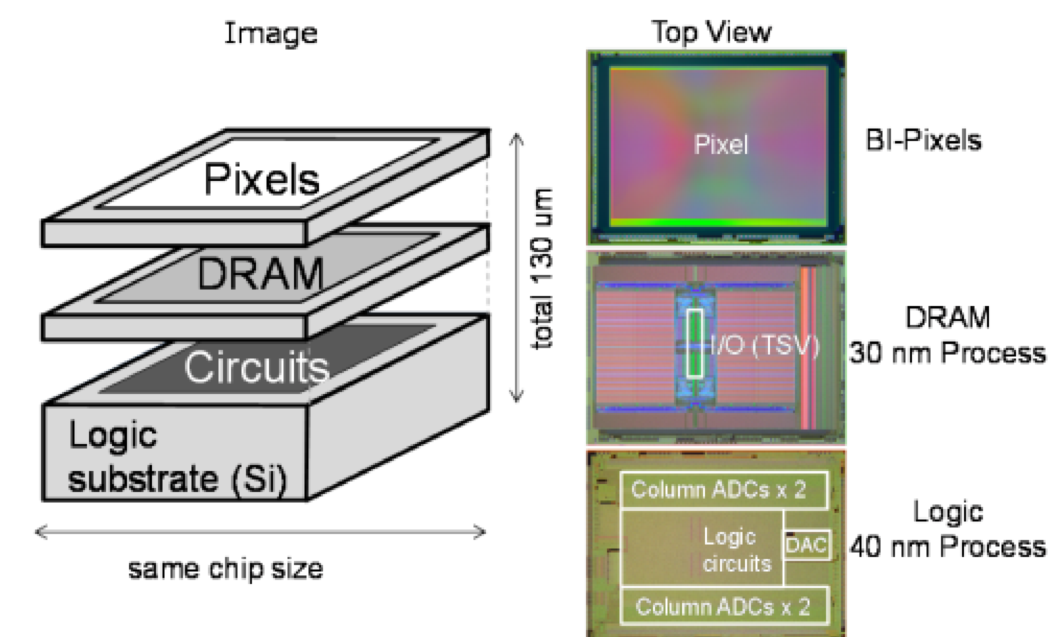
4. Integrates new functions, leading to
Application-Specific Smart Sensors

Features	Benefits	Applications
• Spare area to include IPs	• Application-specific embedded functions • Enables differentiation • Relaxes requirements at system level	• Artificial intelligence • Embedded systems on chip
• Plug & Play IPs	• SERDES, MIPI interface • On-chip micro-controllers/processors	• Ultra-compact systems • Cost sensitive applications

3D stacked technology for CMOS image sensors

What opportunities, performances, & functionalities are enabled by 3D stacking?

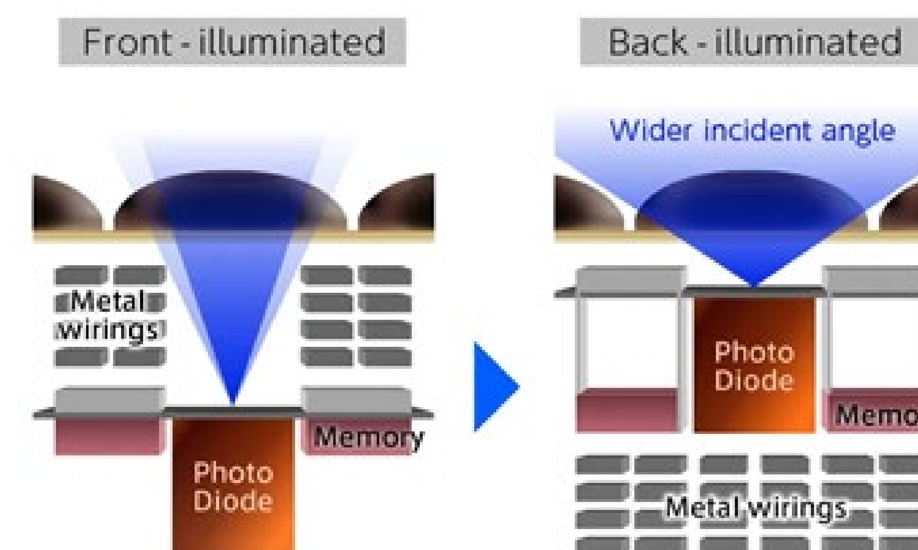
5. Mixing processes and technologies



Features	Benefits	Applications
• Logic in advance technology node	• Image processing • High-speed SERDES	• Artificial Intelligence • Embedded systems on chip • High-speed imaging
• Logic wafers dedicated for memories	• Image processing	• Artificial intelligence
• Logic wafers for communication	• Optical and Rx communications	• Wireless, very high-speed sensor interfaces
• 3 stacked layers (under development)	• Higher integration capabilities	• Concept Camera-on-Chip

3D stacked technology for CMOS image sensors

What opportunities, performances, & functionalities are enabled by 3D stacking?



6. Benefits from Back-Side Illumination technology

Features	Benefits	Applications
• Lower RC time constant	• Increases the speed of control and readout lines	• High-speed image sensor
• Increases number of output lines	• Allows to increase the output bandwidth	• High-speed image sensor
• Improves fill factor	• Increases the sensitivity	• Machine vision, lowlight applications
• UV sensitivity enhancement	• Reduces required emitted light (if active illumination)	• Scientific image sensors
• Scattering structures +DTI	• NIR improvement and lower cross talk	• Scientific image sensors

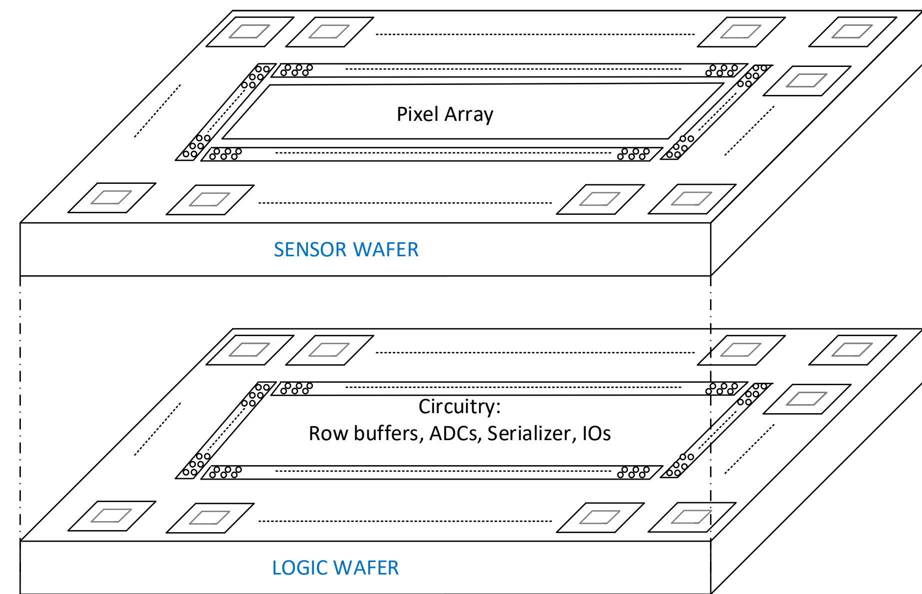
3D stacked technology for CMOS image sensors

Process details & sensor floorplan

For BSI-stacked, wafers will consist of 2 layers: sensor wafer & logic wafer

Sensor wafer

Will contain mainly pixels, via areas to interconnect with the logic wafer and aluminum pads for bonding wires

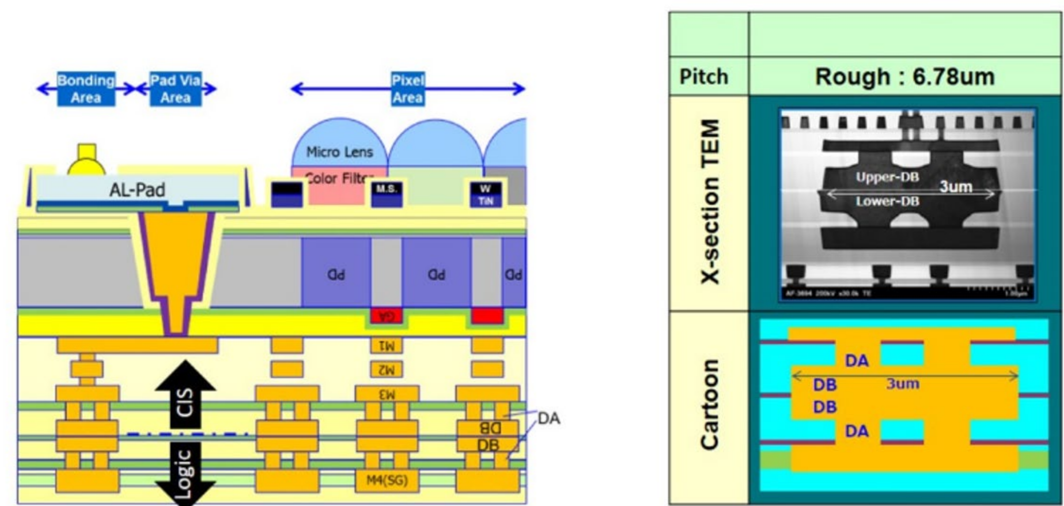


Logic wafer

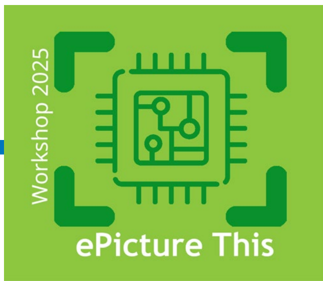
(Up to 8 metals, SRAM layer, DMOS or MIM for capacitors) contains all mixed-signal elements to operate the pixel, digitize, and output data

Process options:

- Epi Thickness maximizing QE in the wavelengths of interest
- Deep Trenches Isolation (DTI): full/partial or dual DTI
- TSV and/or Cu-to-Cu hybrid



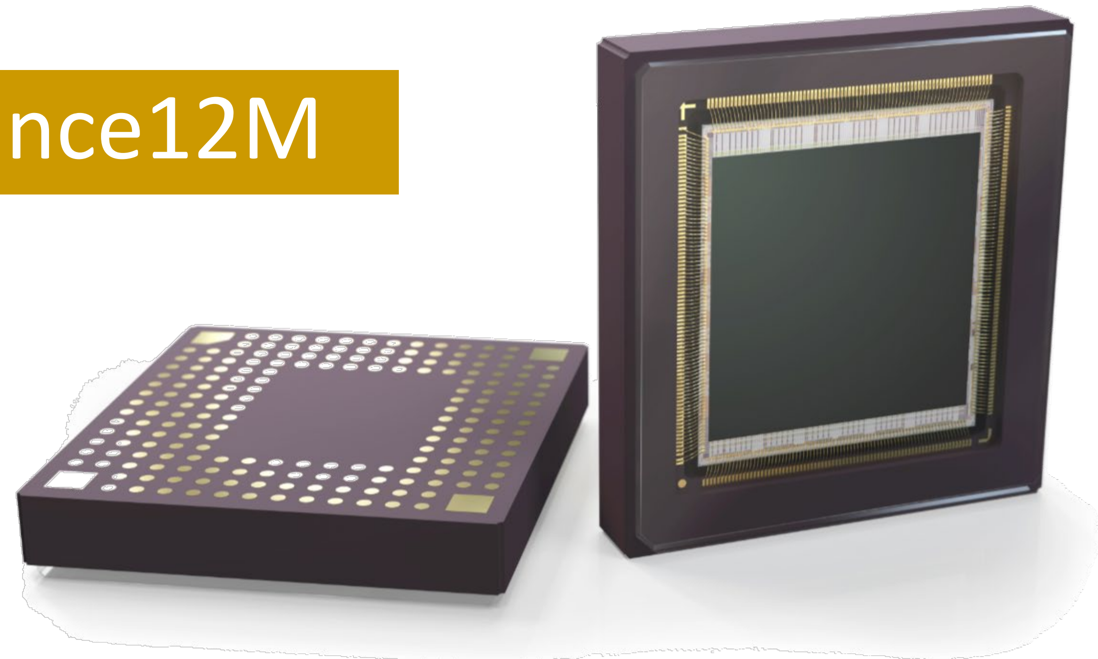
- Readout, pixel array selection, & interface circuitry
- Serialize the data & deliver to IO ports
- IO ESD protection included at this level
- Several technology options: 65nm & 40nm



3D stacked technology for CMOS image sensors

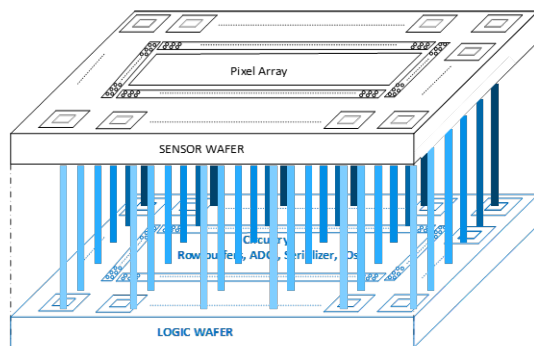
Ongoing developments at Teledyne e2v

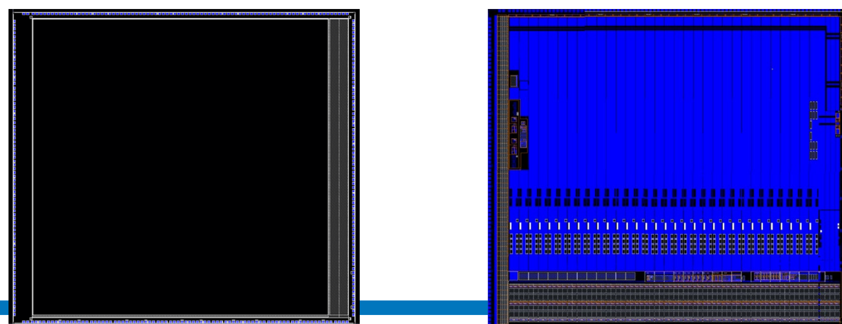
Lince12M



- ✓ 3.2µm Global Shutter pixel BSI with DTI
- ✓ High frame rate thanks to a distributed, 2D array of ADCs and digital circuitry
- ✓ HDR feature in pixel
- ✓ On-chip digital pre-processing functions reducing computational power of further AI algorithms
- ✓ Only 235µm periphery area (PADs)

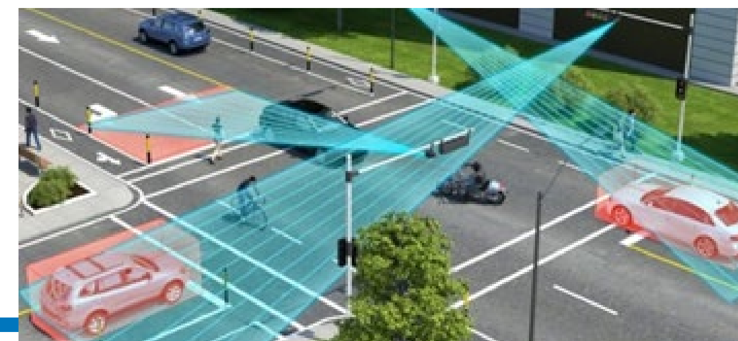
Layout

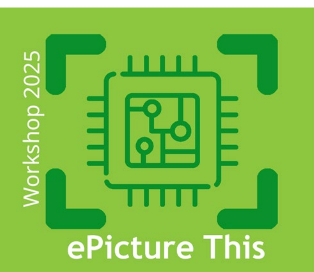




Applications

- ✓ Machine Vision
- ✓ ITS, HDR
- ✓ Medical





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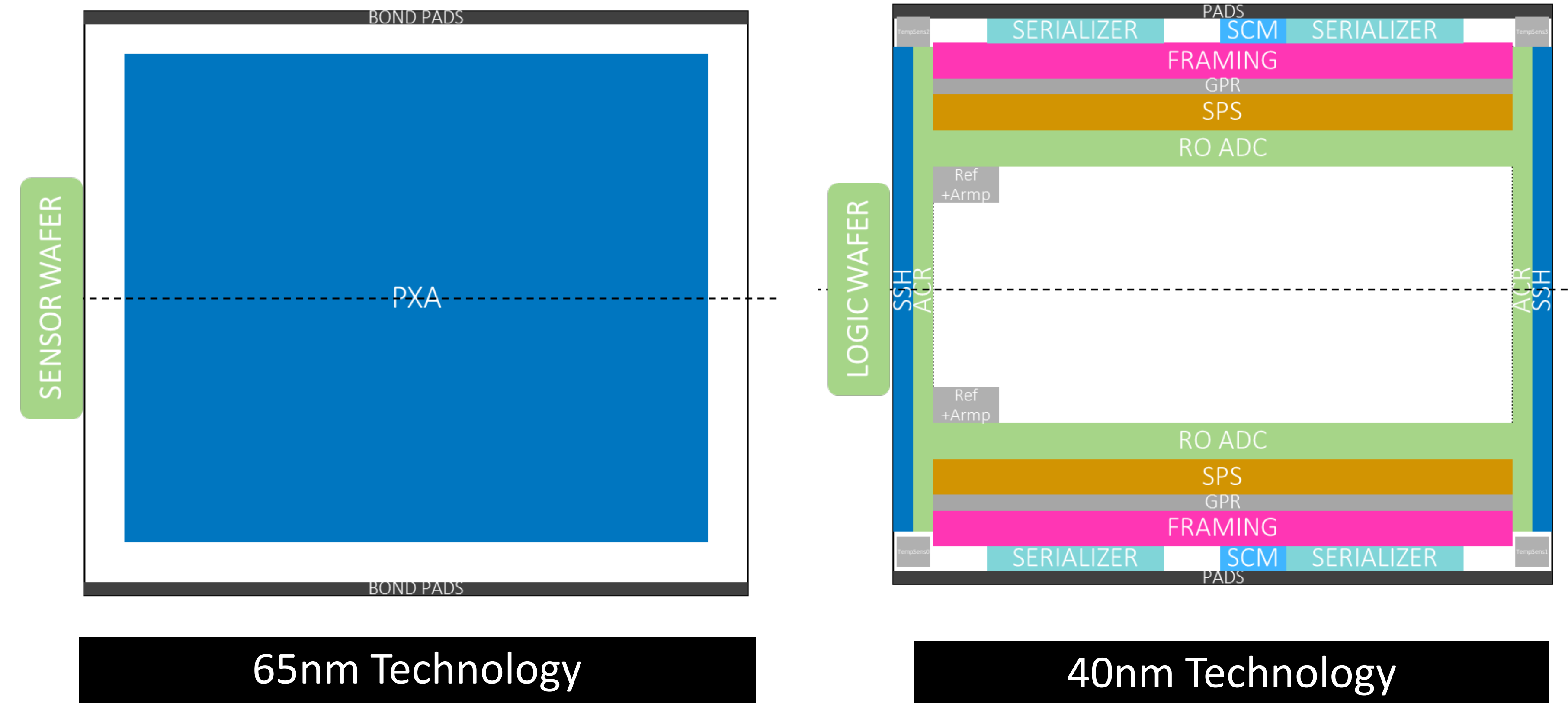
Organized by projects: 2021004 Imagination (Penta)
2023022 Elevation (Xecs)
2024001 Entertain (Xecs)

3D stacked technology for CMOS image sensors

Ongoing developments at Teledyne e2v

Ultra high-resolution sensor @100fps (STM)

- ✓ BSI thick EPI (NIR)
- ✓ +5Gbps CML ports
- ✓ Redundant digital circuity to improve yield
- ✓ 2W Power consumption

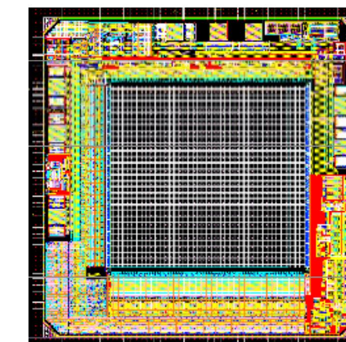


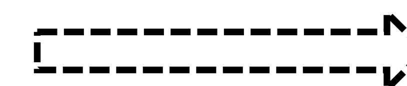
65nm Technology

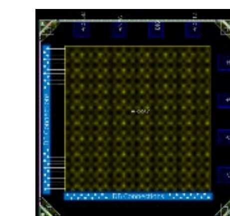
40nm Technology

High sensitivity 1.1mm² sensor (TPSCo)

- ✓ Low noise
- ✓ +100fps
- ✓ 40mW





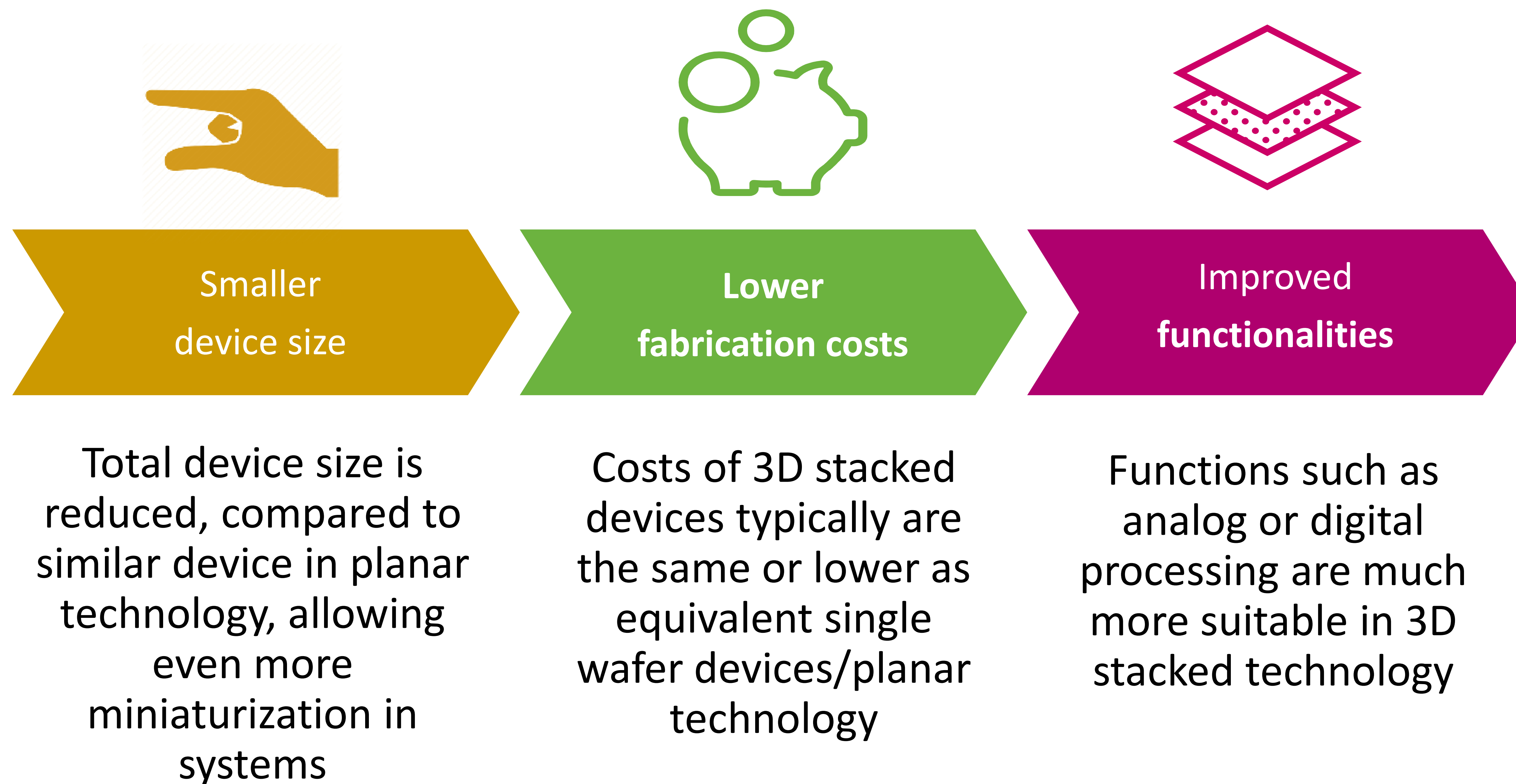


Front side, single layer

3DS

3D stacked technology for CMOS image sensors

Very convenient for image sensor developments



3D stacked technology for CMOS image sensors

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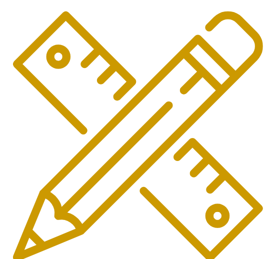
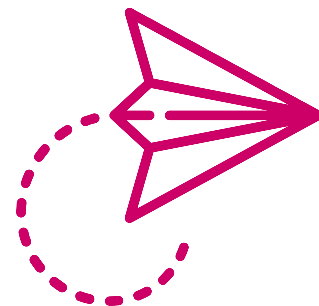
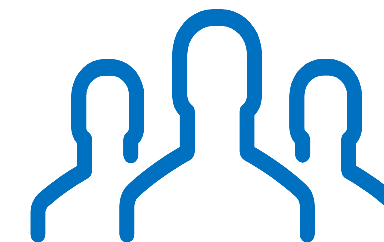
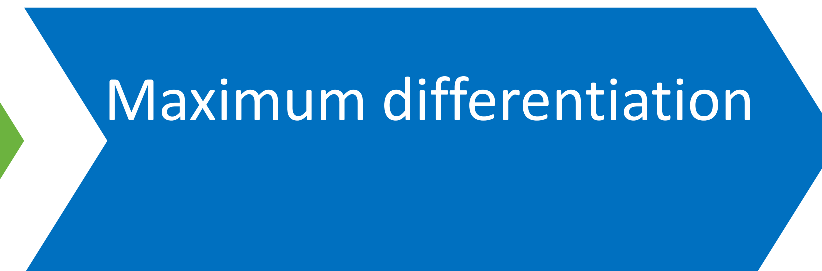


BSI pixel design, performances, & technology such as full trenched DTI, scattering structures, multiple memory nodes are directly incorporated

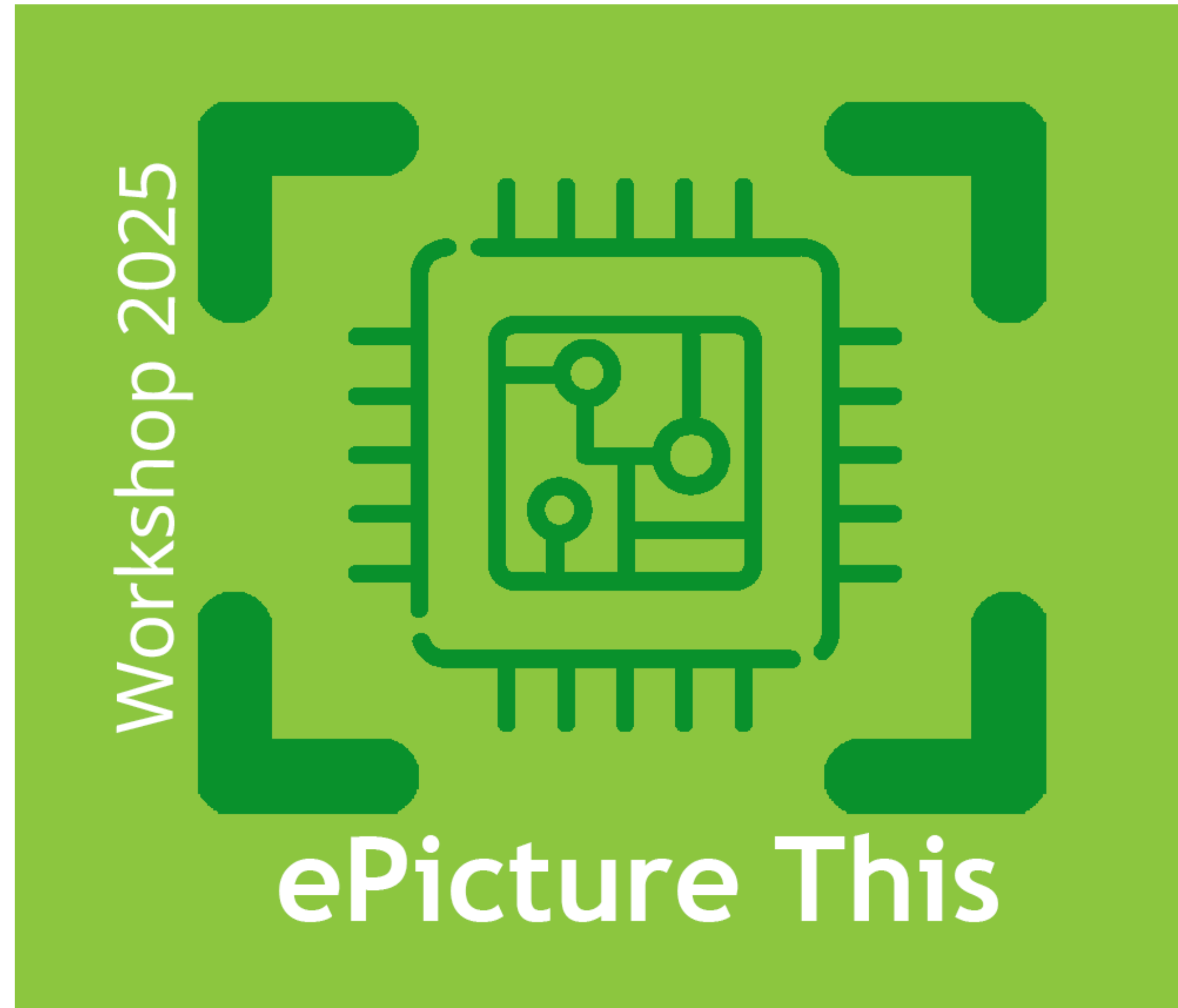


Teledyne e2v currently has six projects under development & new opportunities coming

3D stacked technology with **three layers** is under development, offering even better functionalities, improvements, & optimizations, such as high density memories or DSP

3D stacked technology provides customers with maximum differentiation & enables new sensor families, targeted for specific applications



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