Post-Processing the Future of Imaging: Towards Broadband CMOS Image Sensors

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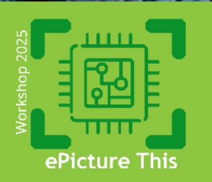
Eindhoven, the Netherlands

28th October, 2025

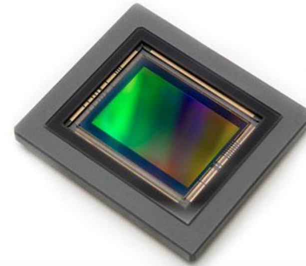


Organized by projects: 2021004 Imagination (Penta)
2023022 Elevation (Xecs)
2024001 Entertain (Xecs)

Outline

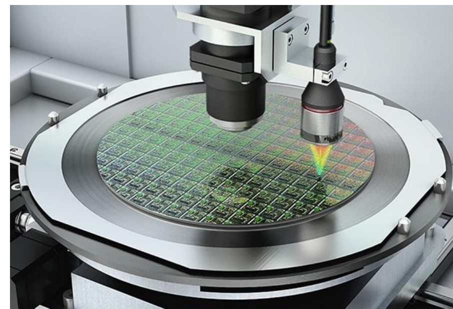
- ★ Si based CMOS image sensors
- ★ Integration challenges for broadband CMOS image sensors
- ★ Post-processing technique for broadband CMOS image sensors
- ★ Preliminary results from post-processing of Si photodiodes
- ★ Key takeaways and future direction

CMOS Image Sensors: The Eyes of Modern Technology

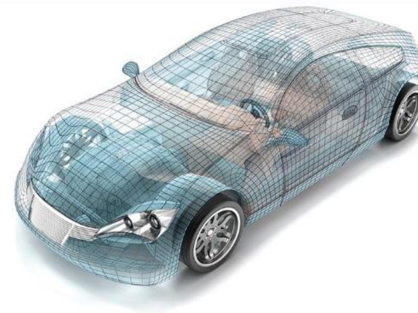


Fun fact: Around 6.8 billion units of CMOS image sensors produced worldwide in 2023

Consumer Electronics



Industrial & Machine Vision

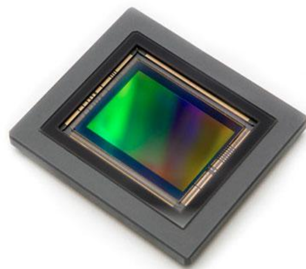


Automotive & Mobility

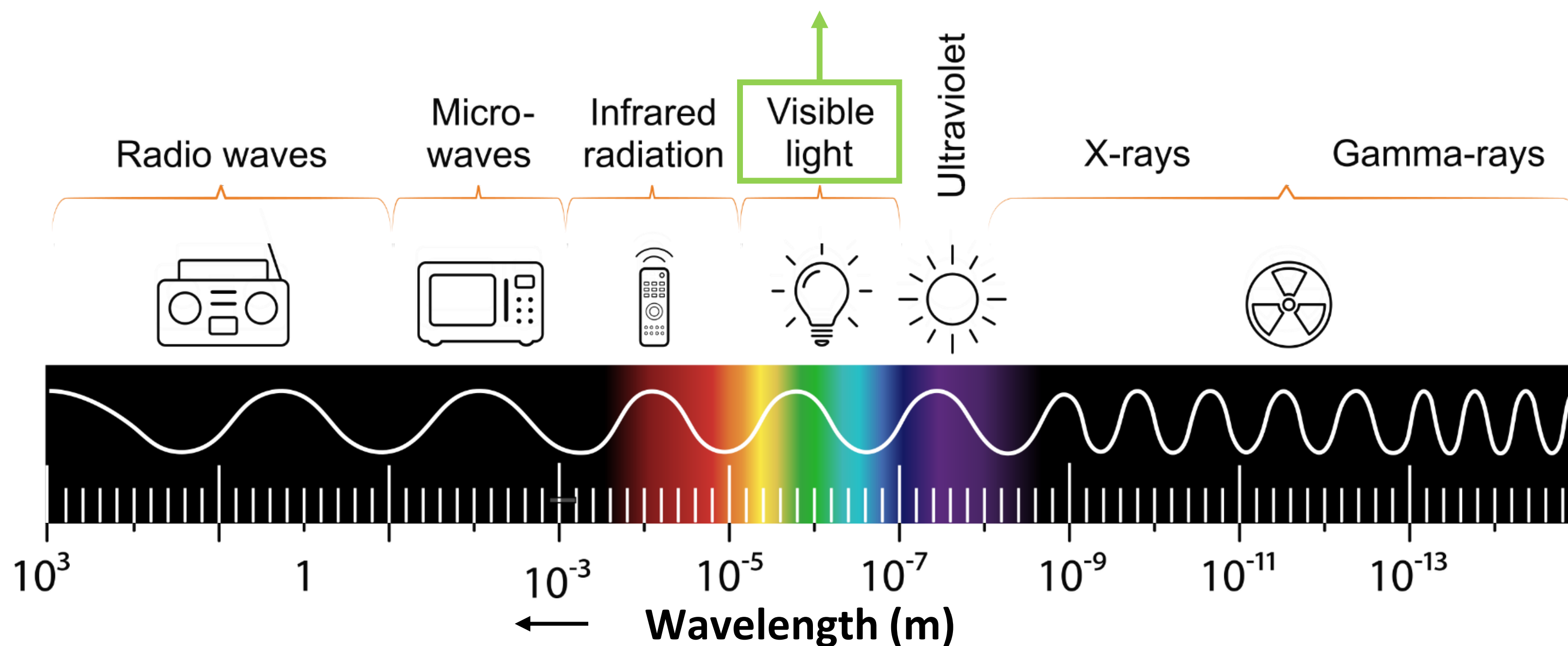
Security & Surveillance

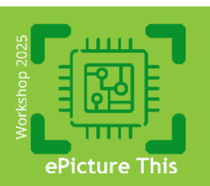
Source: [EE World]

CMOS Image Sensors: The Eyes of Modern Technology



Si-based CMOS image sensors





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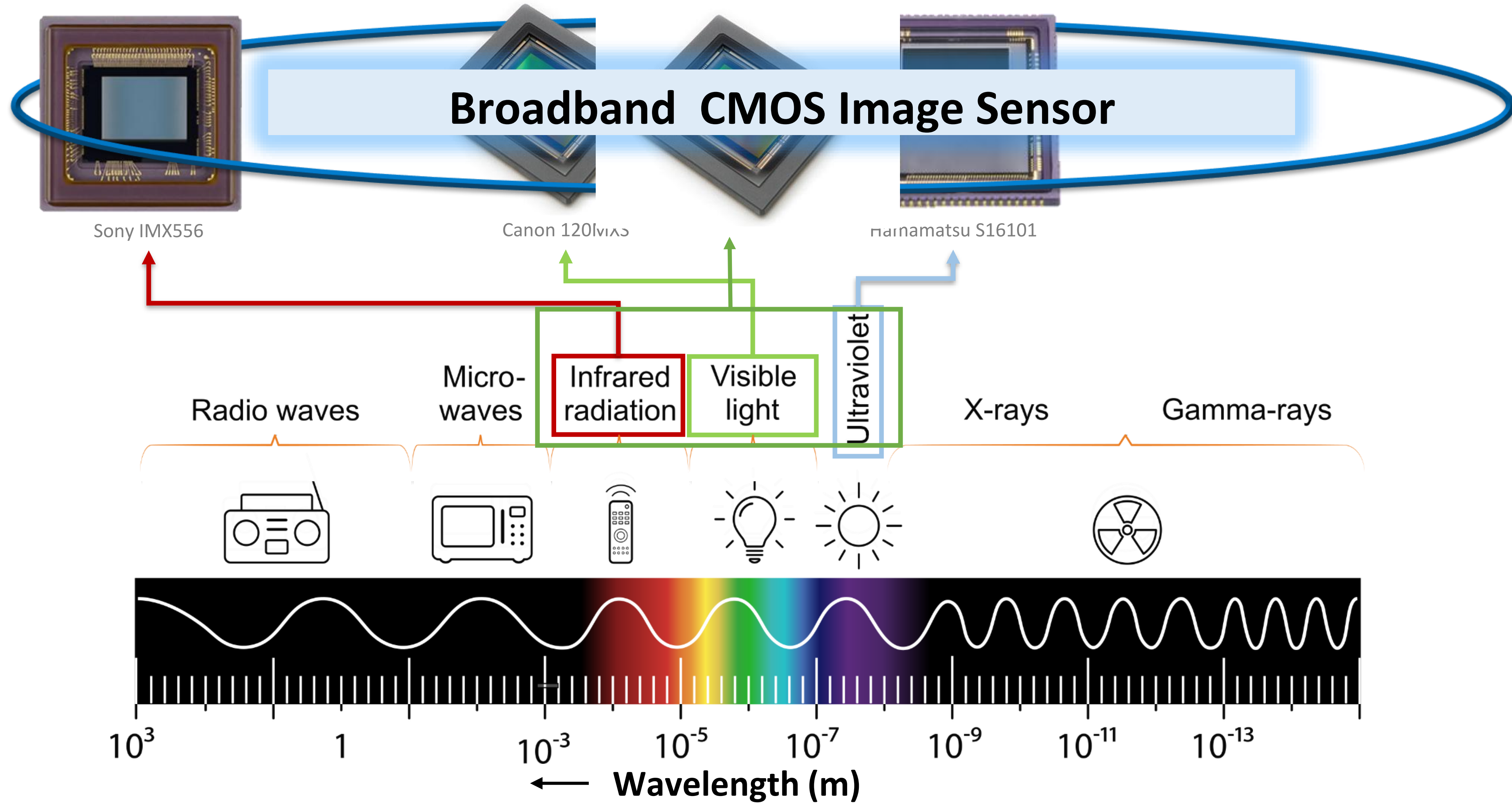
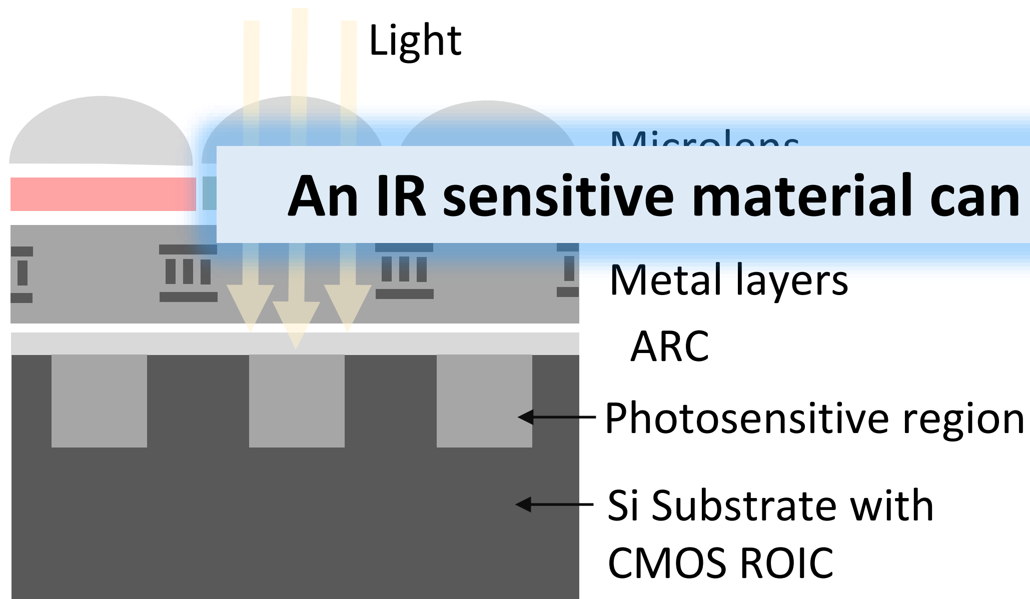
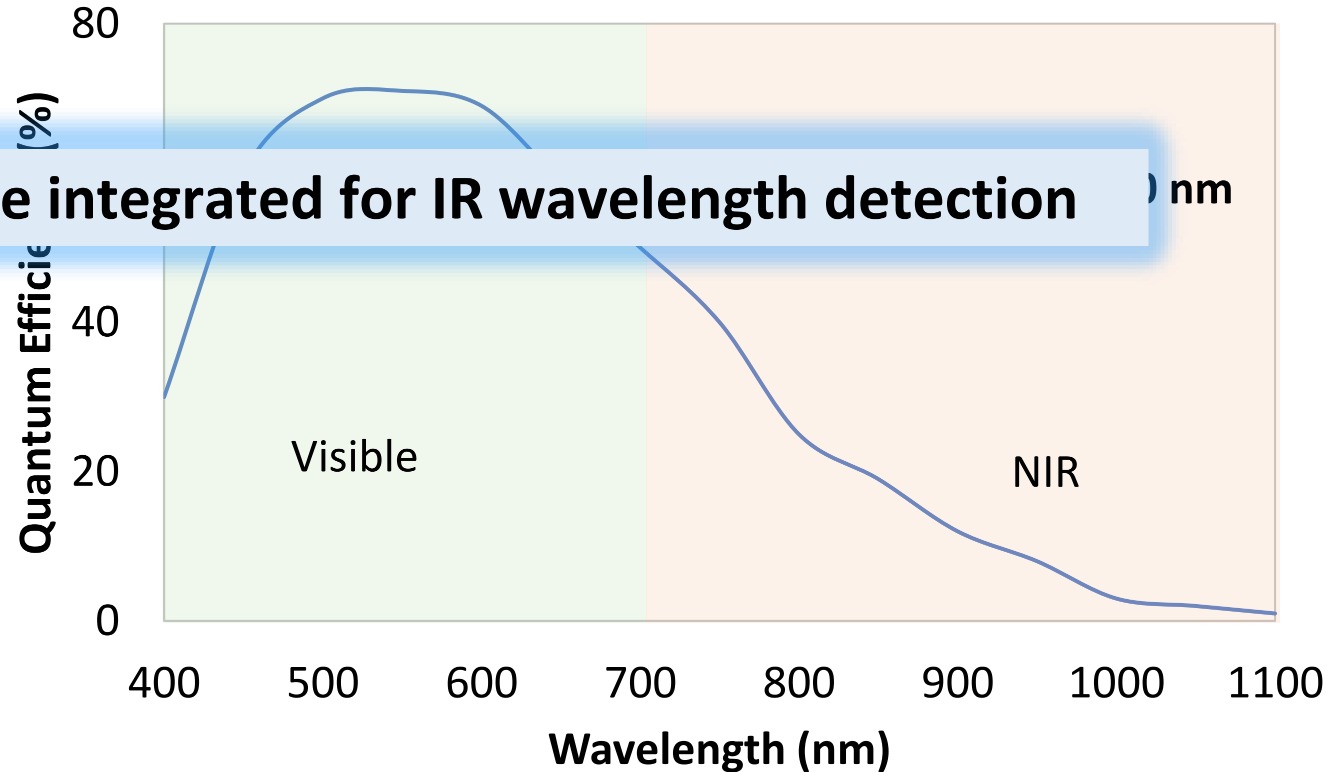
Broadband CMOS Image Sensors



Si CMOS Image Sensors: Limitations



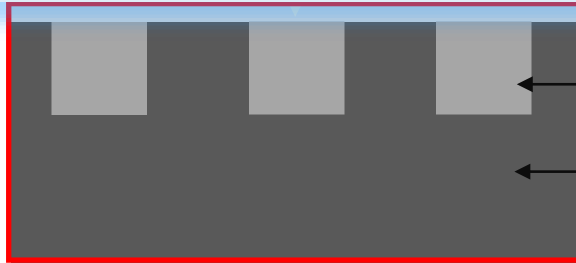
Si-based CMOS image sensors



An IR sensitive material can be integrated for IR wavelength detection

ARC: Anti-reflective coating

The Integration Challenge: IR materials vs CMOS Compatibility



Si-based CMOS image sensors

Maintain CMOS compatibility

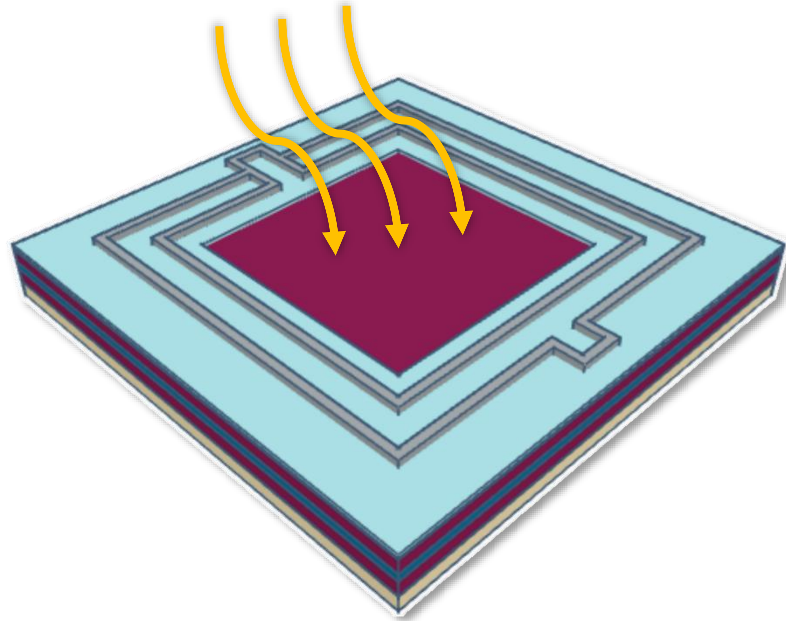
ıt-end-of-line (FEOL): Formation of
sistors and junctions

ng a new material (IR-sensitive) in FEOL
ədesigning the whole foundry process

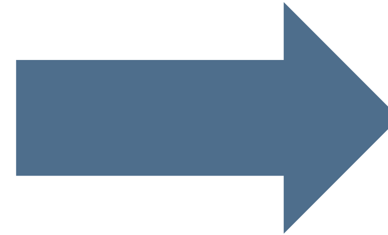
A Smarter Approach
Post-Processing of Si CMOS Image Sensors

A Smarter Approach: Post-Processing of Si CMOS Image Sensors

Visible only detection

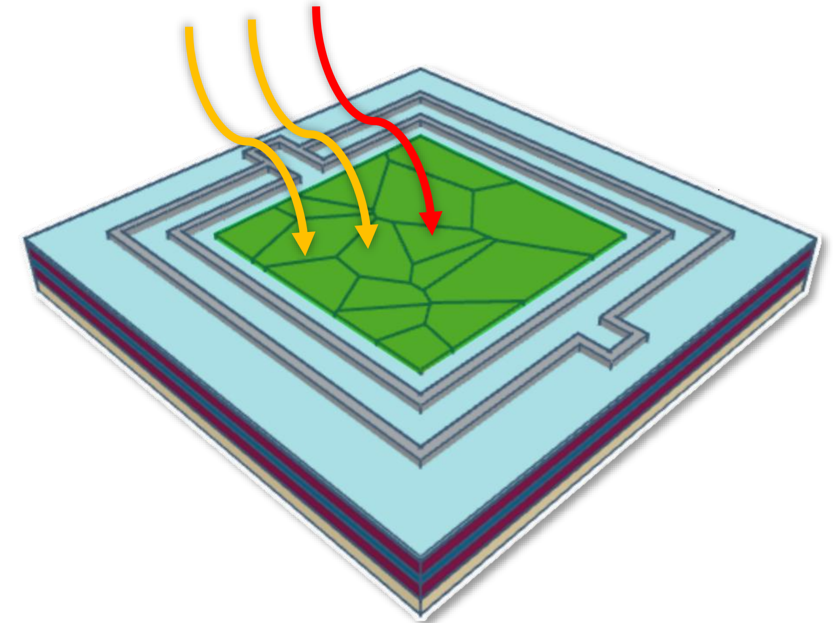


Si CMOS Image Sensor



Low-temperature post-processing step*

Visible + SWIR only detection



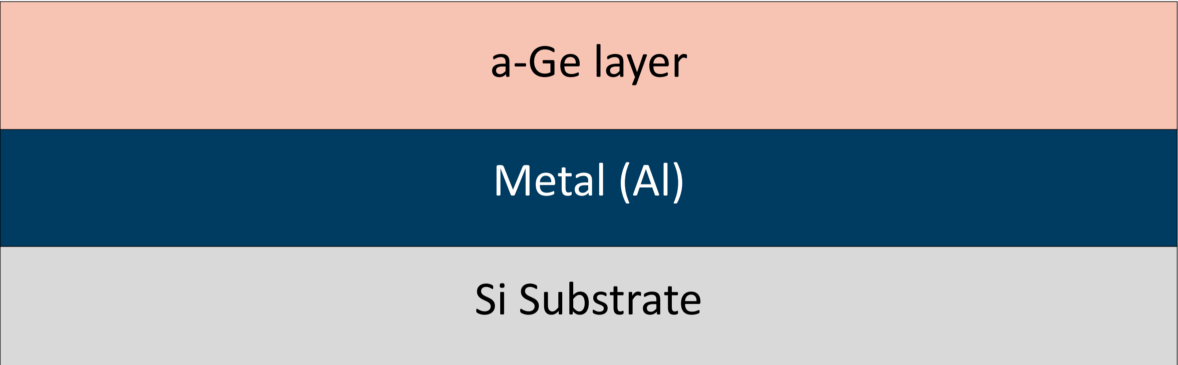
IR sensitive + Si CMOS Image Sensor

*to comply with BEOL thermal limits ≤ 350°C

Layer Exchange Process: Post-Processing Step

Low temperature growth of crystalline semiconductor material

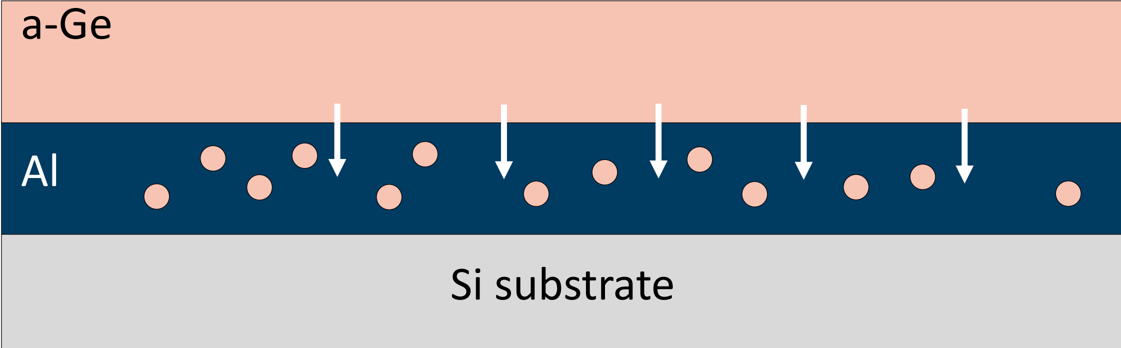
Step 1: Sputtering of metal (Al) and amorphous Ge layer



Layer Exchange Process: Post-Processing Step

Low temperature growth of crystalline semiconductor material

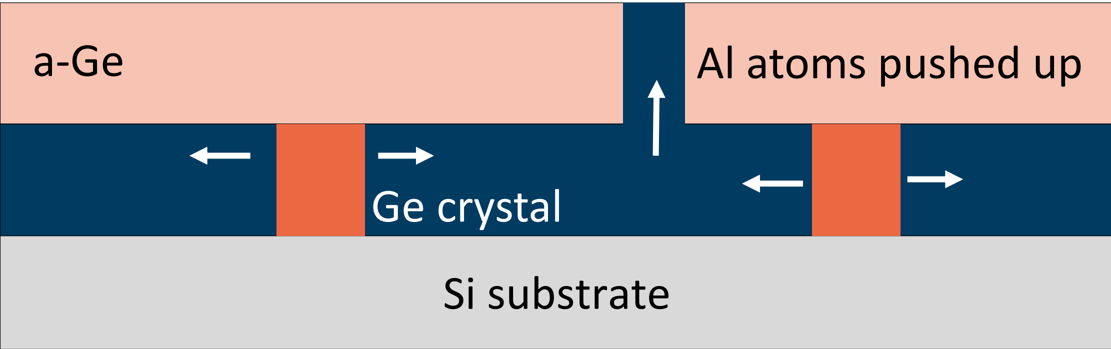
Step 2: Annealing (@350°C for 25 hrs)



Layer Exchange Process: Post-Processing Step

Low temperature growth of crystalline semiconductor material

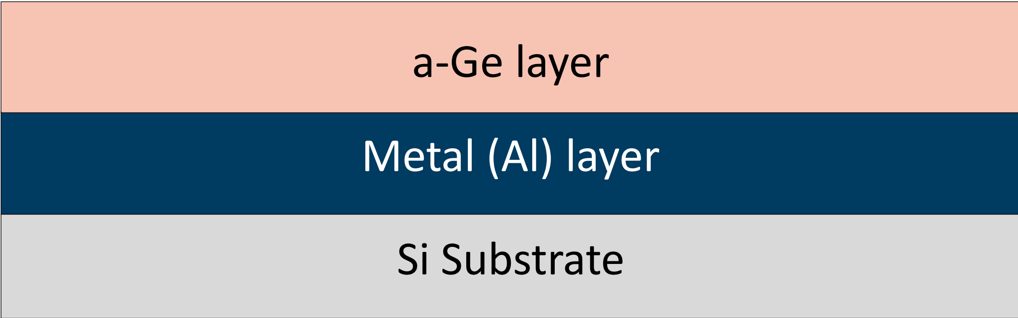
Step 3: Nucleation and lateral growth of Ge crystals during annealing



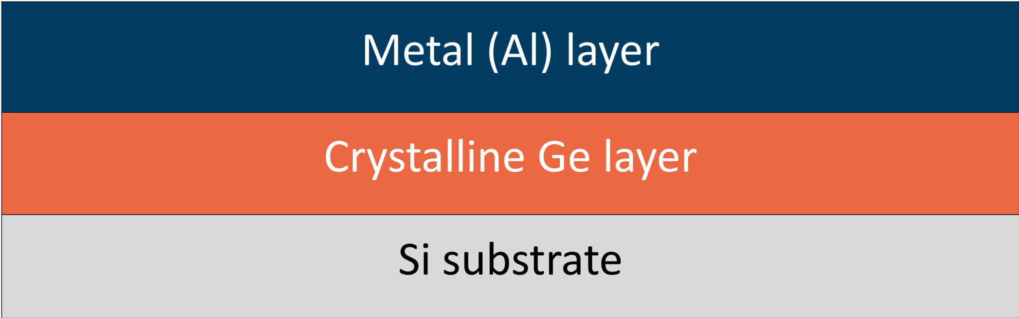
Layer Exchange Process: Post-Processing Step

Low temperature growth of crystalline semiconductor material

Step 4: Complete exchange of layers



Before annealing

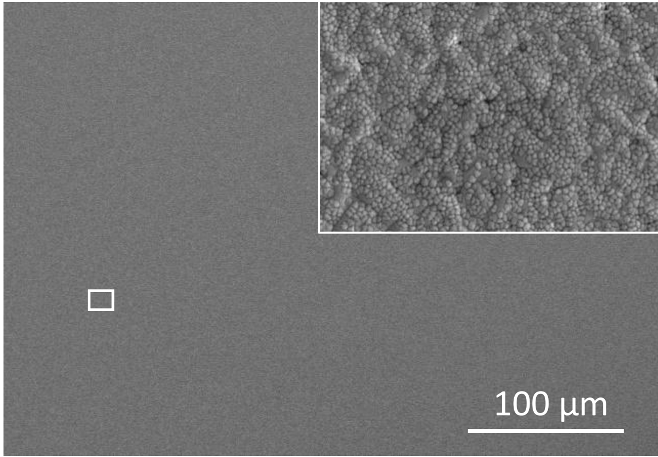


After annealing

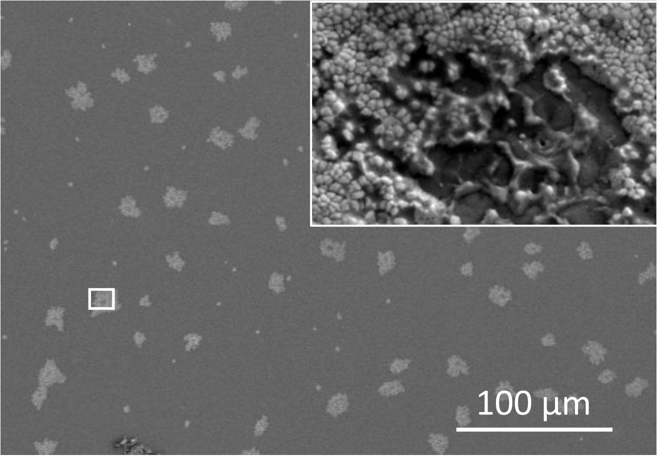
Layer Exchange of Ge/Al on Si

SEM analysis

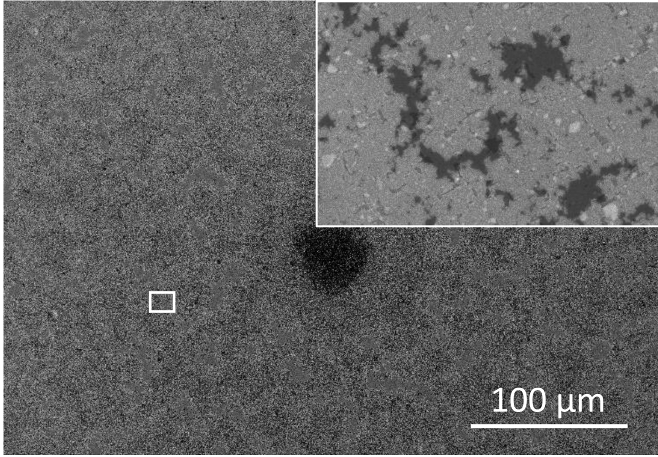
Sample: Ge (50 nm)/ Al (50 nm) on Si substrate



Before annealing



After 5 hours of annealing @350°C



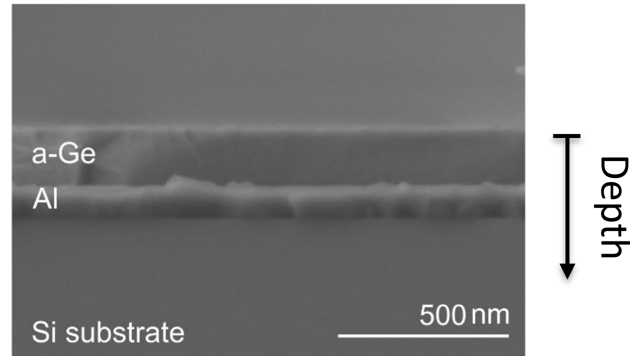
After 25 hours of annealing @350°C

SEM: Scanning Electron Microscope

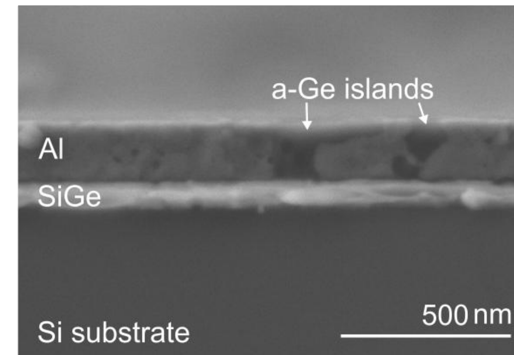
Layer Exchange of Ge/Al on Si

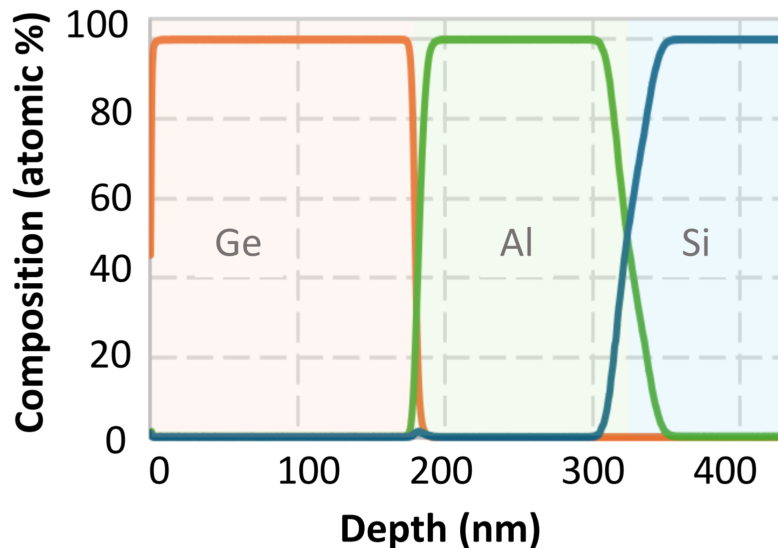
SIMS Analysis

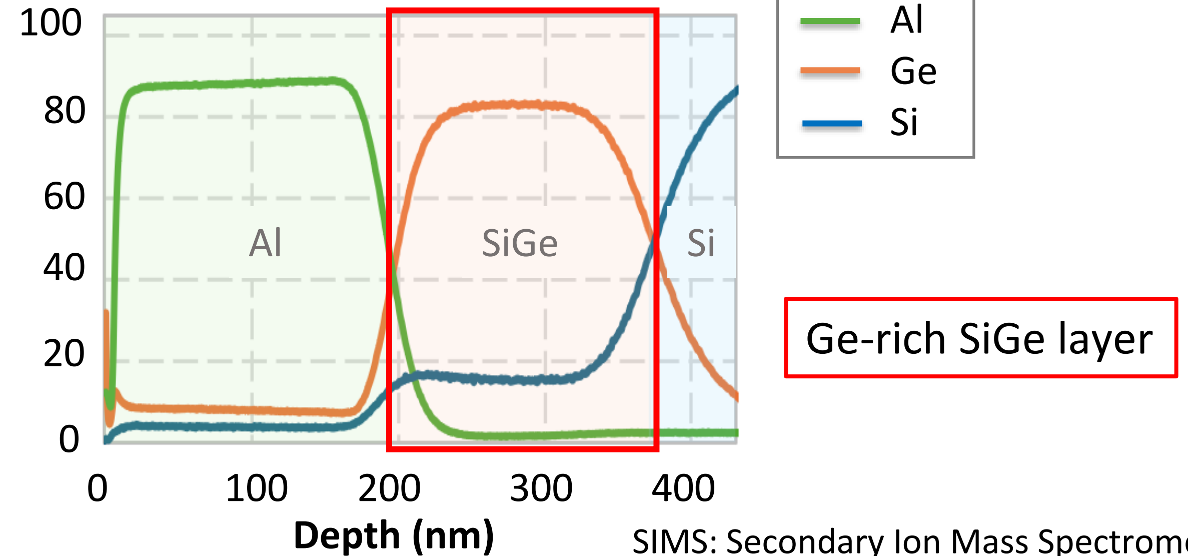
Before annealing



After 25 hours of annealing @ 350°C



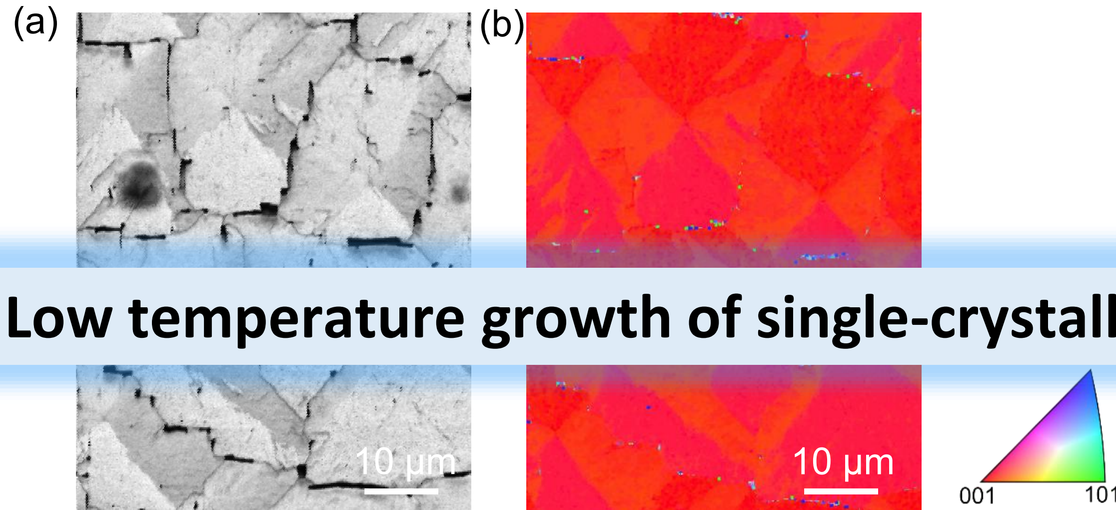




SIMS: Secondary Ion Mass Spectrometry

Layer Exchange of Ge/Al on Si

EBSD Analysis



Average grain size (µm)	(100)-oriented %
[illegible]	99.5

Low temperature growth of single-crystalline Ge (100) on Si substrate

EBSD analysis: (a) Grain size and (b) crystal orientation of the top c-Ge layer after layer exchange and etching the top Al layer

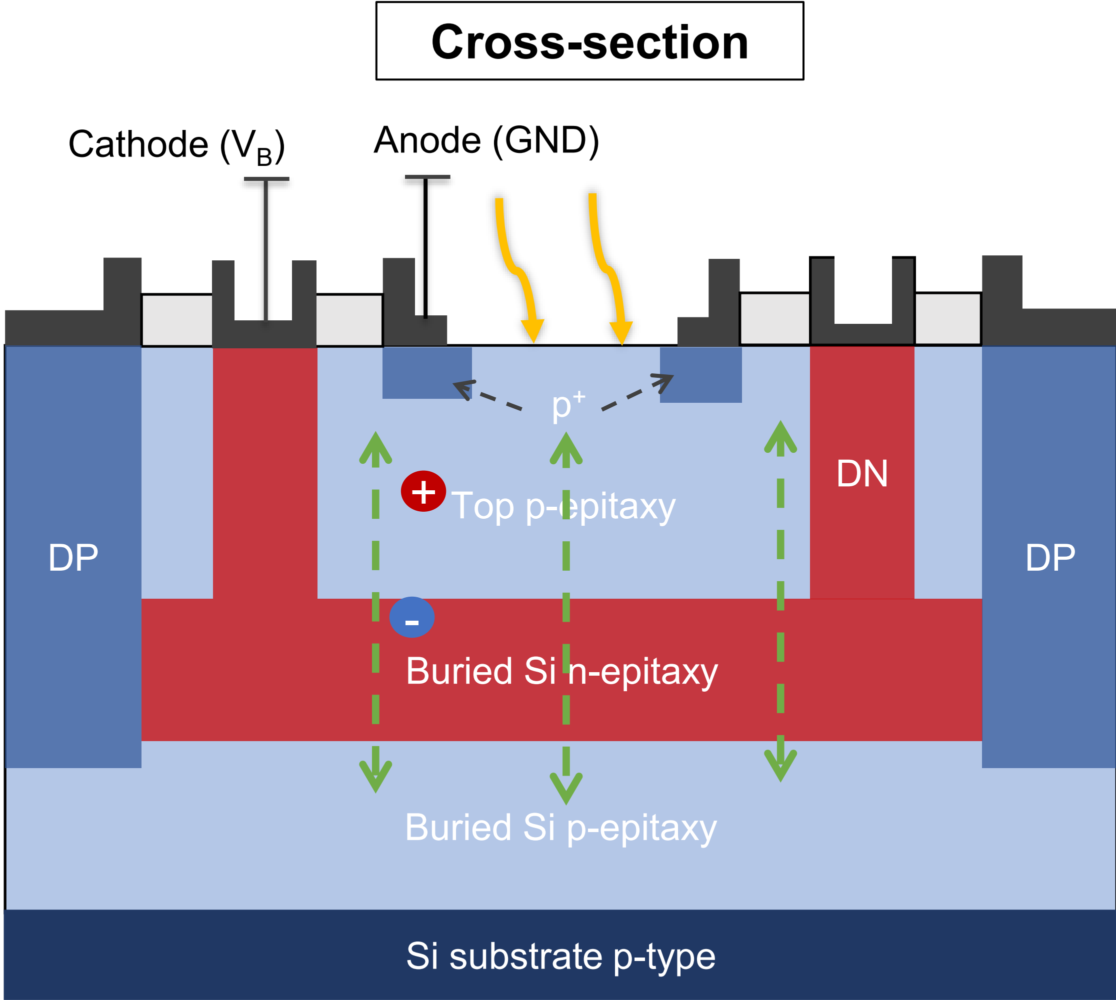
EBSD: Electron Backscatter Diffraction

Transfer of Layer Exchange Technology to Si Photodiodes

Low temperature integration of Ge

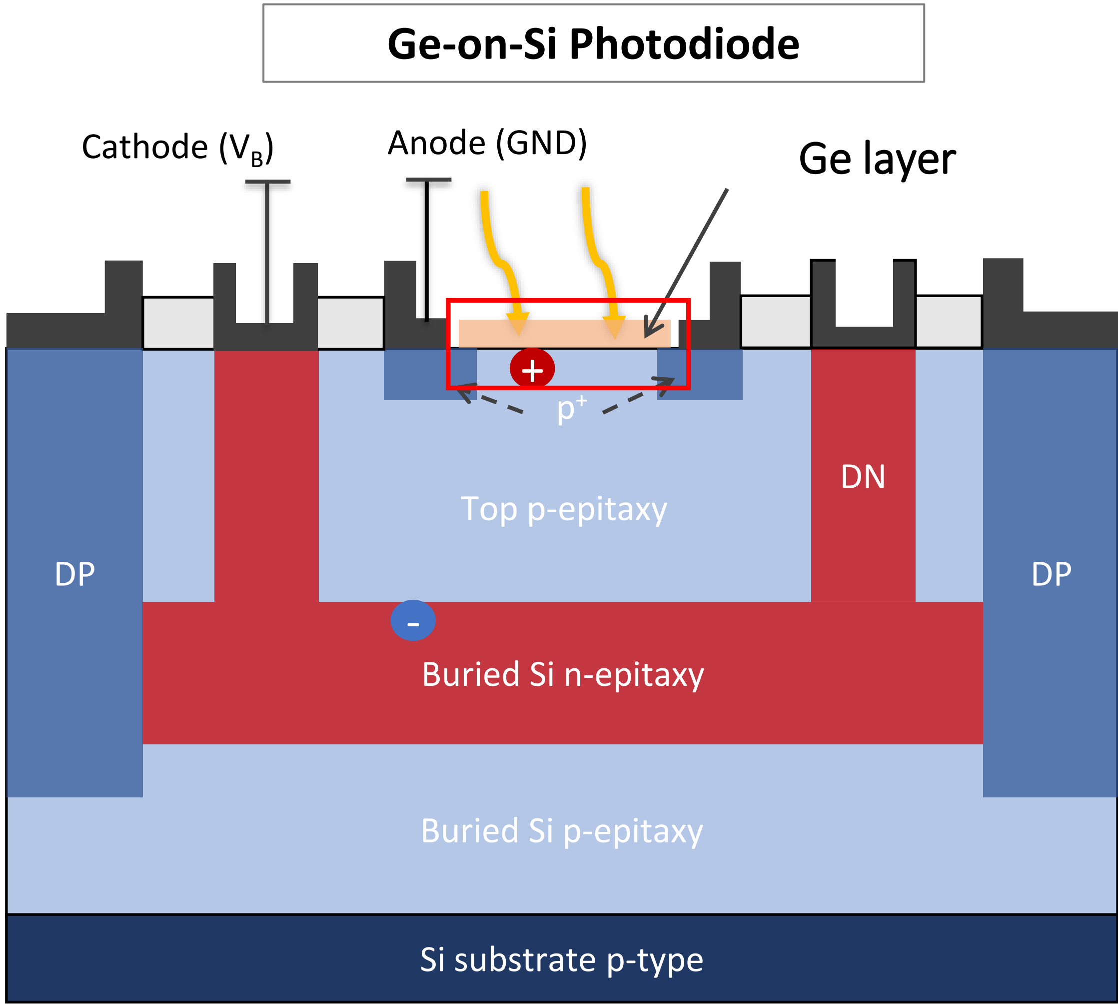
Si Photodiode: Fabrication

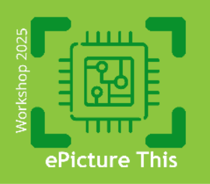
Cross-section



Test device (Si Photodiode) structure

Ge Integration on Si Photodiode



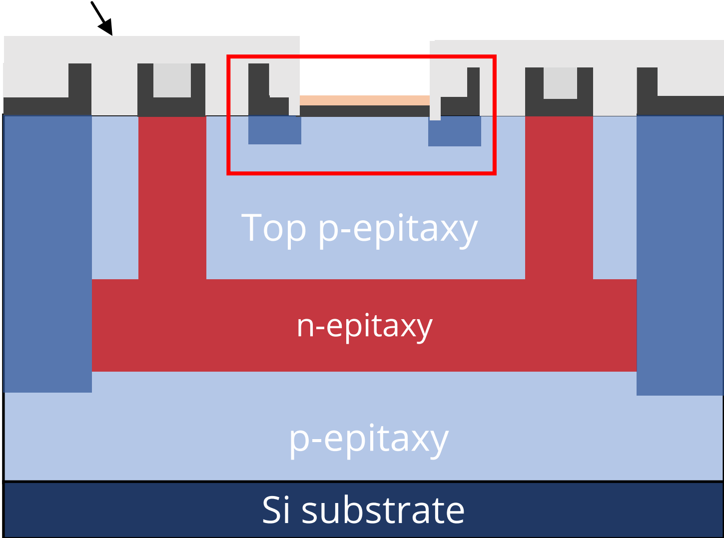


Layer Exchange on Si Photodiode

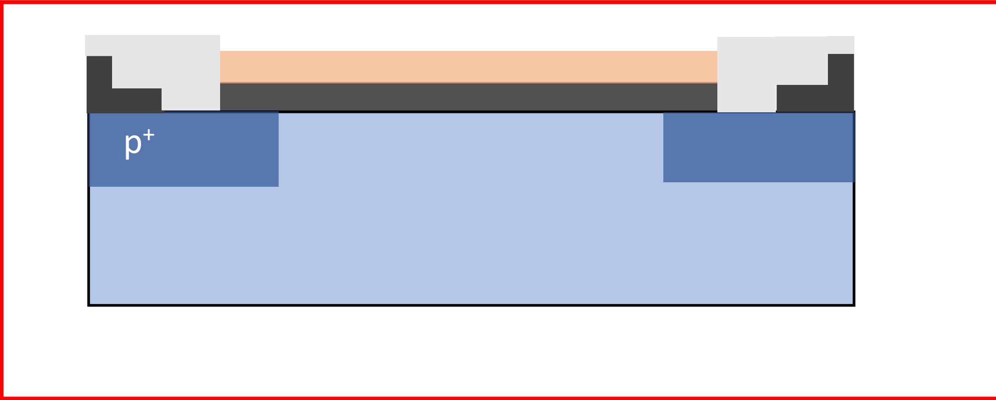
Ge-on-Si Photodiode

Sputtering of Ge/Al stack

SiO_2 (100 nm) to protect metal contacts



Ge/Al layer exchange in the photosensitive region



Layer Exchange on Si Photodiode

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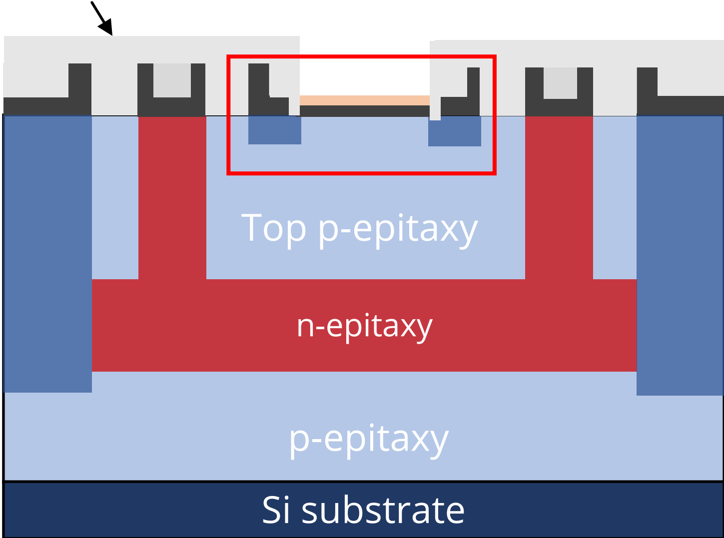
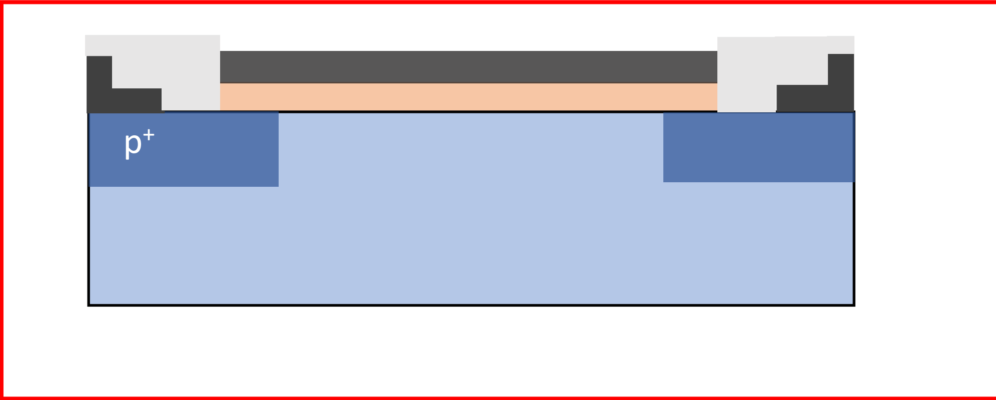
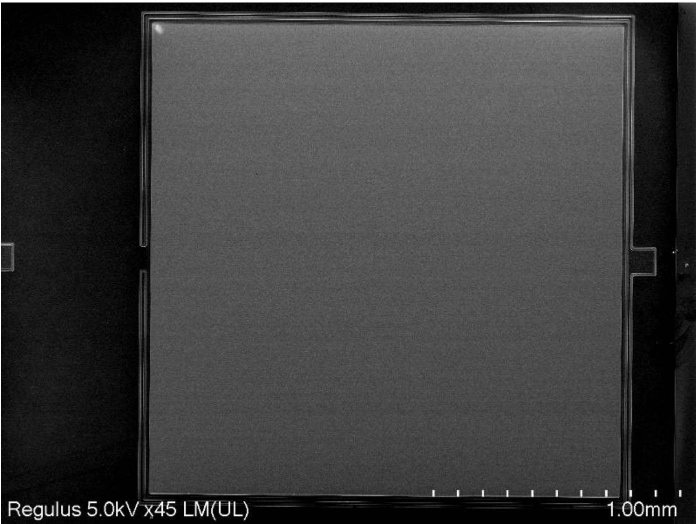


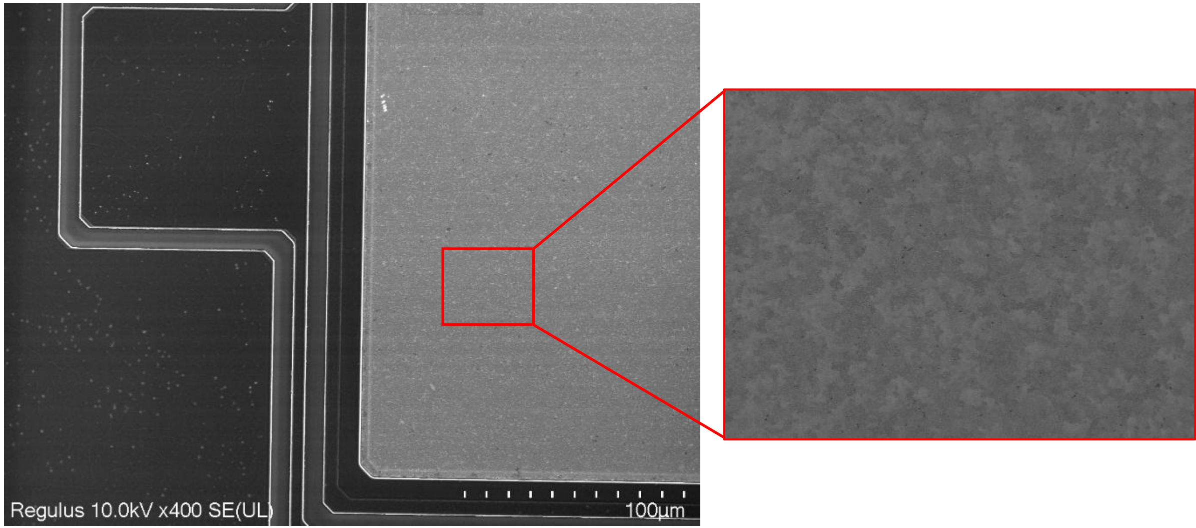
Ge/Al layer exchange in the photosensitive region



Layer Exchange on Si Photodiode

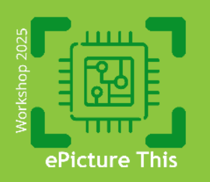
Ge-on-Si Photodiode





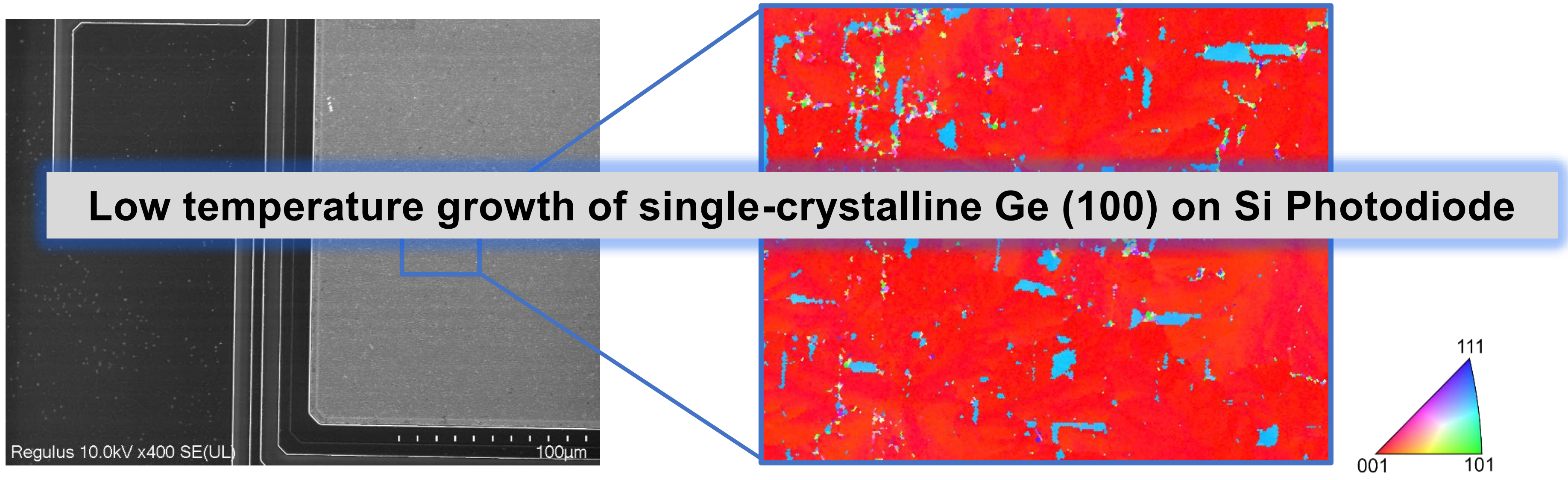
Si Photodiode before layer exchange

Ge-on-Si Photodiode after layer exchange



Layer Exchange on Si Photodiode

Crystal quality of Ge layer

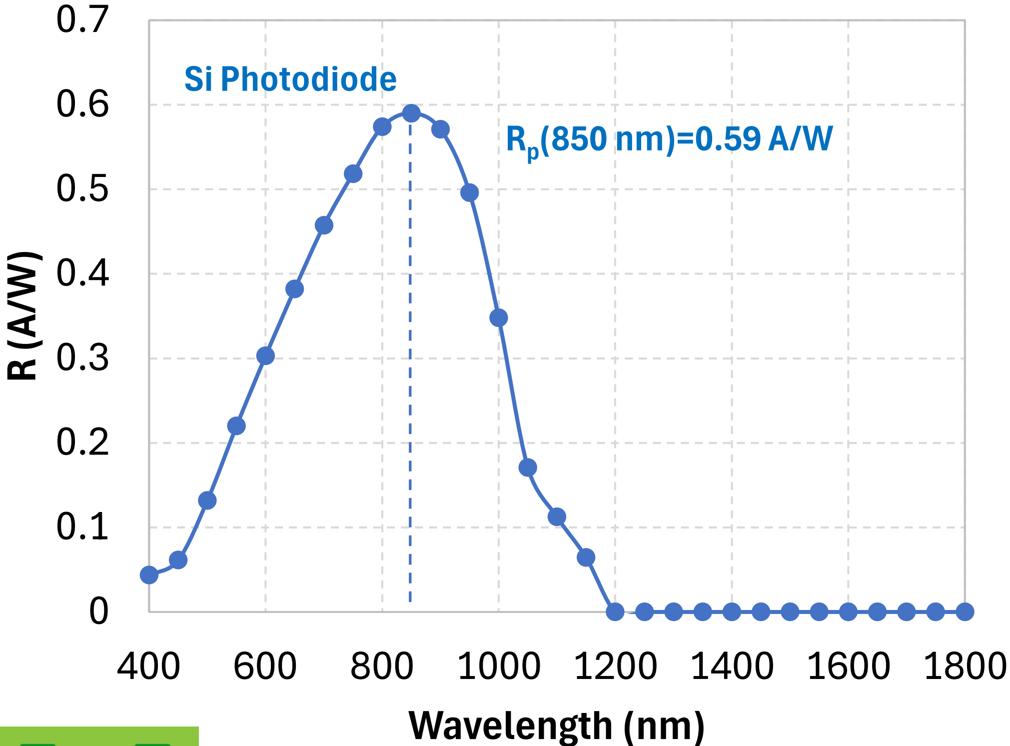


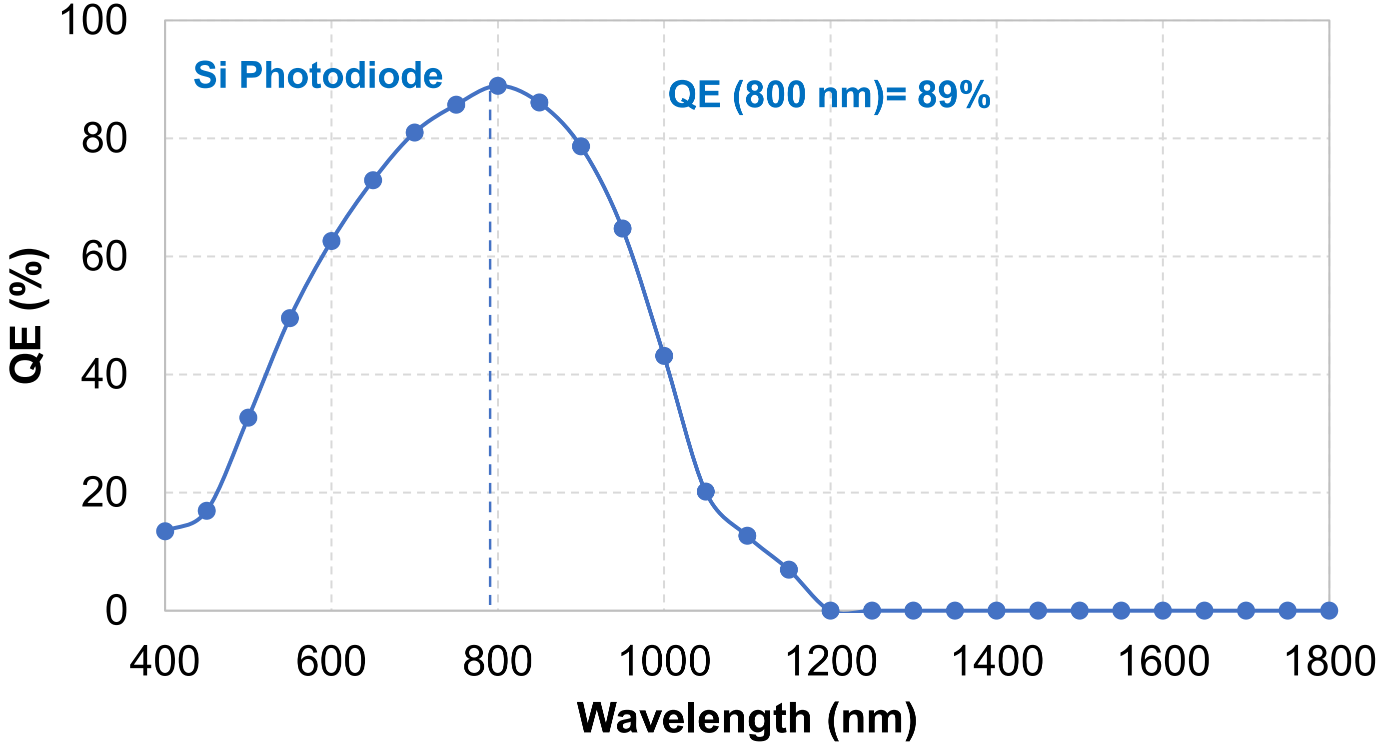
EBSD analysis: Ge layer

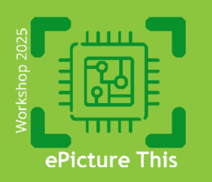
Optical Characterization of Si Photodiode

$$Responsivity = \frac{Photocurrent}{Incident\ optical\ power}$$

$$External\ QE = \left(\frac{R}{\lambda}\right)\frac{hc}{q}$$

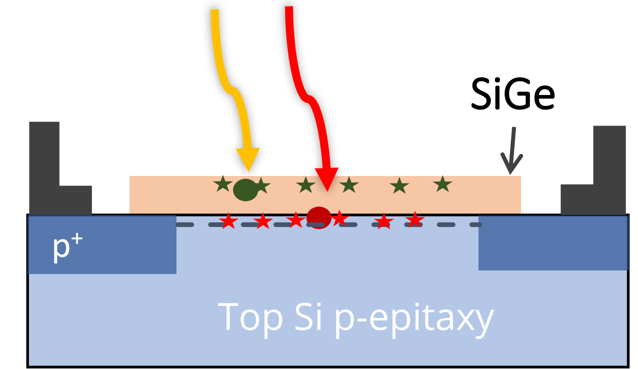


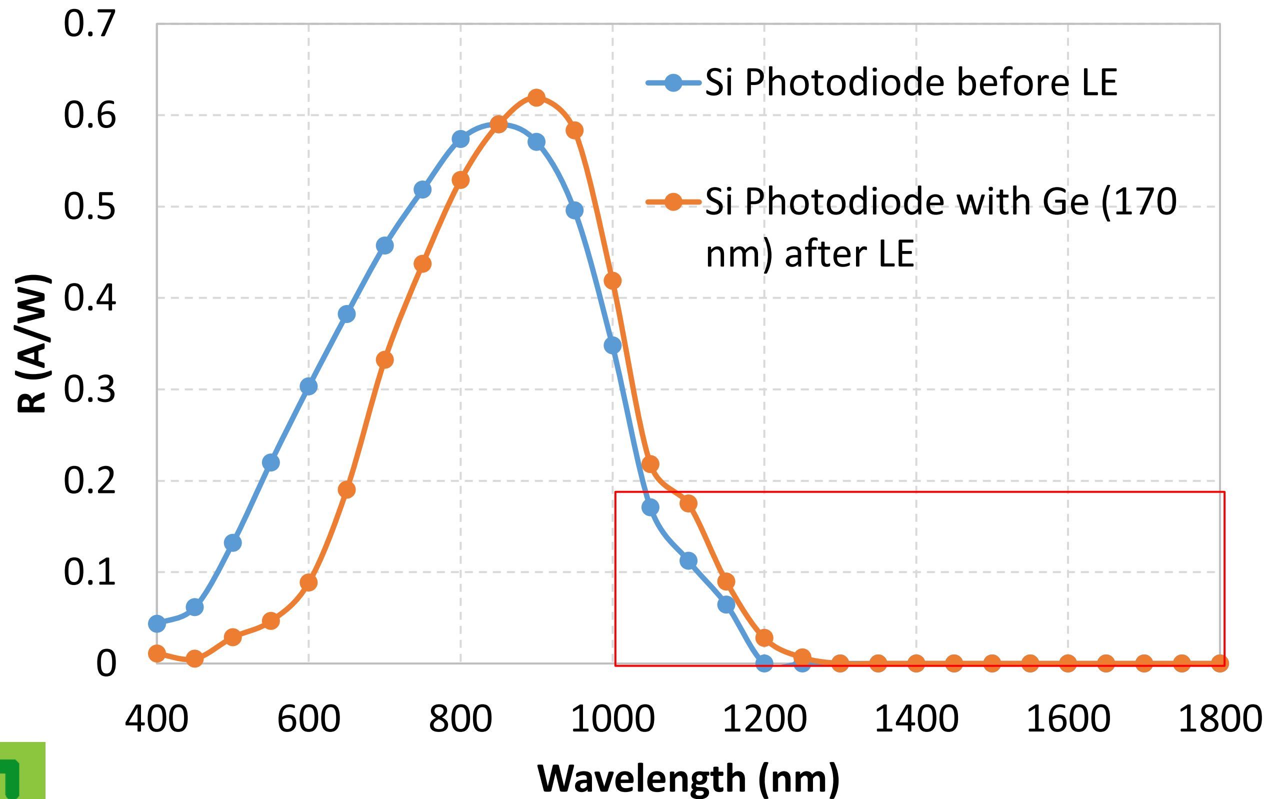


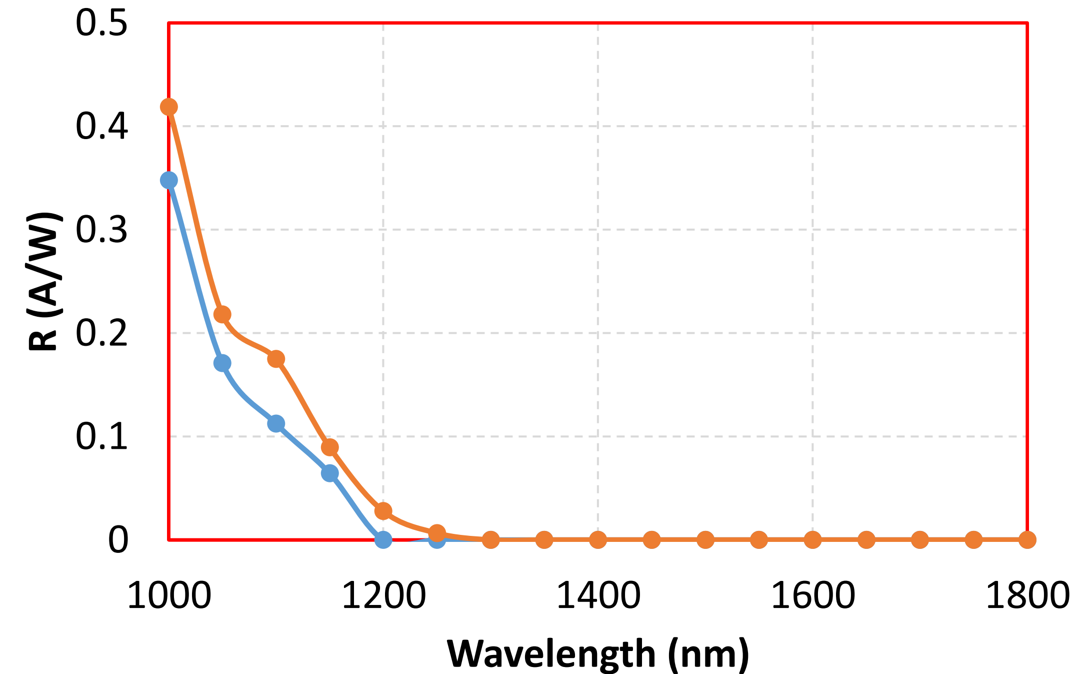


Broadband Response of Ge-on-Si Photodiode

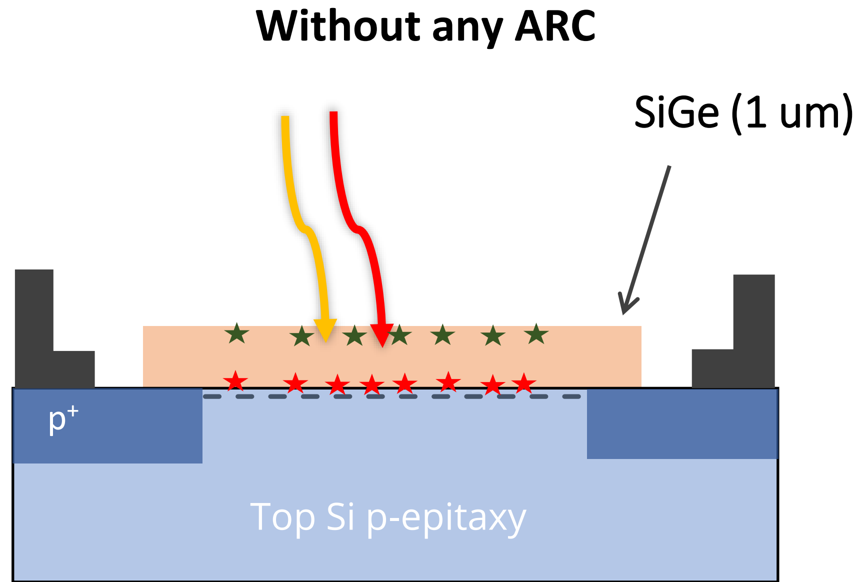
- **Preliminary results:**
  - Photodiode without any passivation and anti-reflective layer
  - SWIR response is limted by thin Ge layer and Si-Ge interface

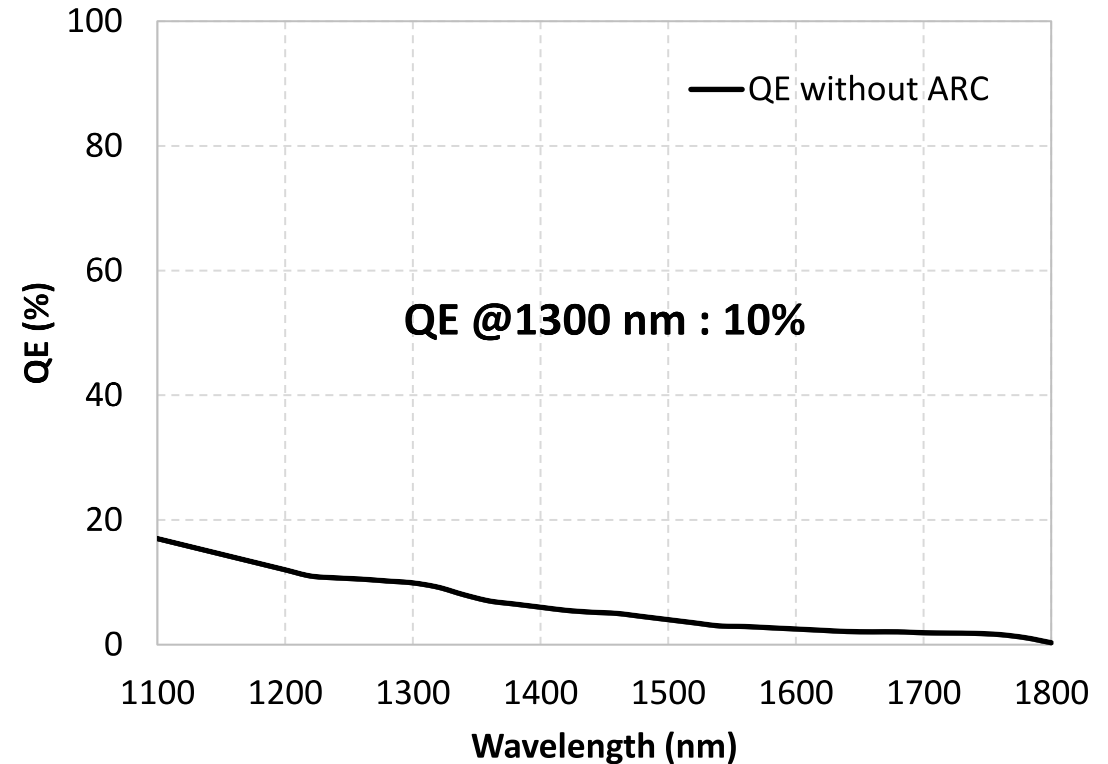






Simulation of Optical Response in Ge-on-Si Photodiode

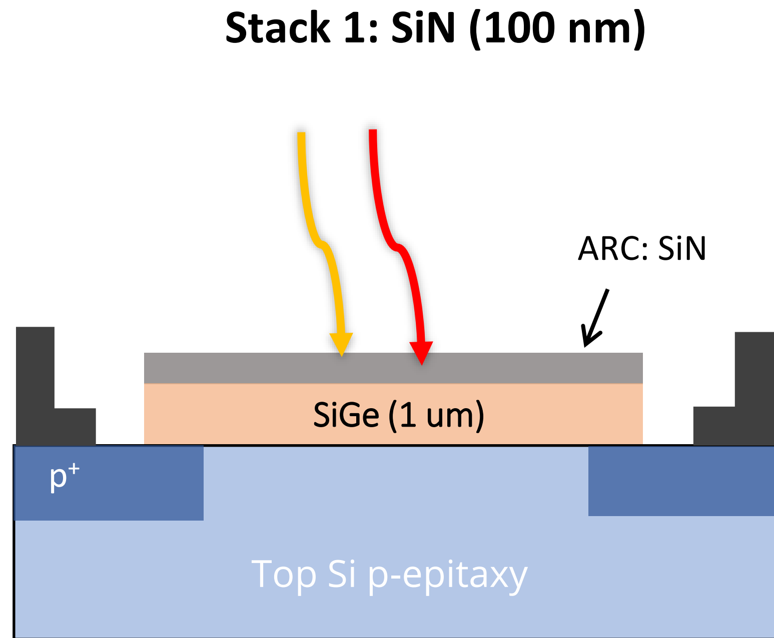


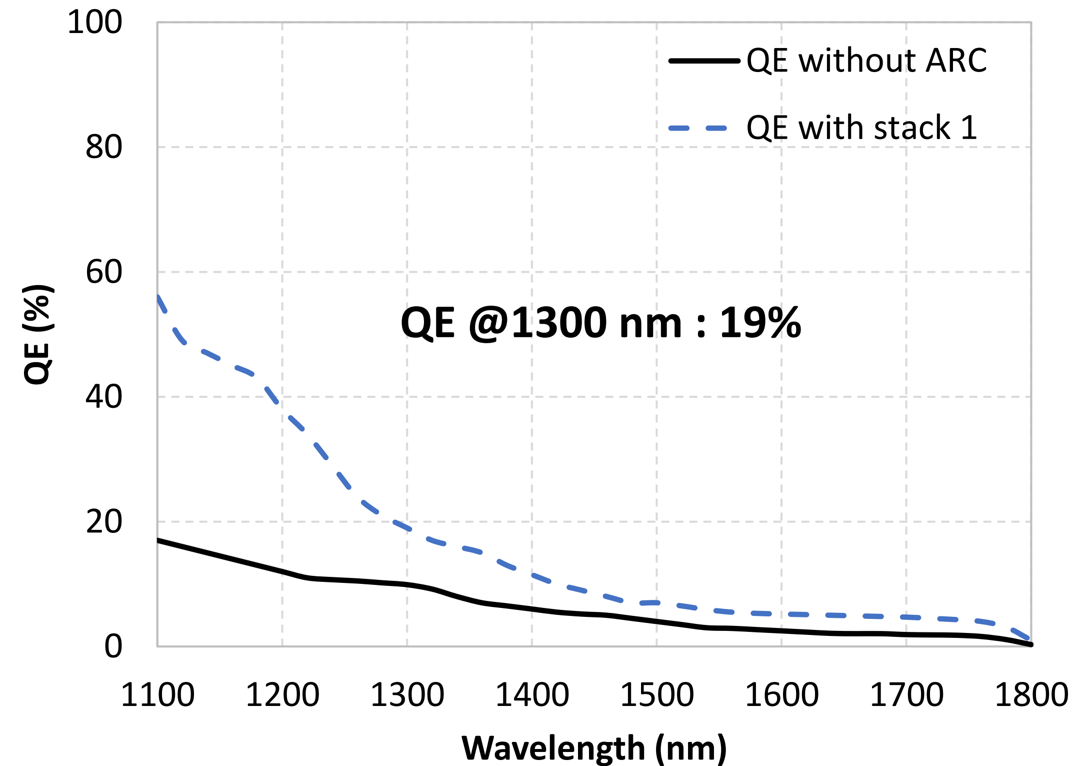


ARC: Anti-reflective Coating

Simulation of Optical Response in Ge-on-Si Photodiode

- With anti-reflective layer



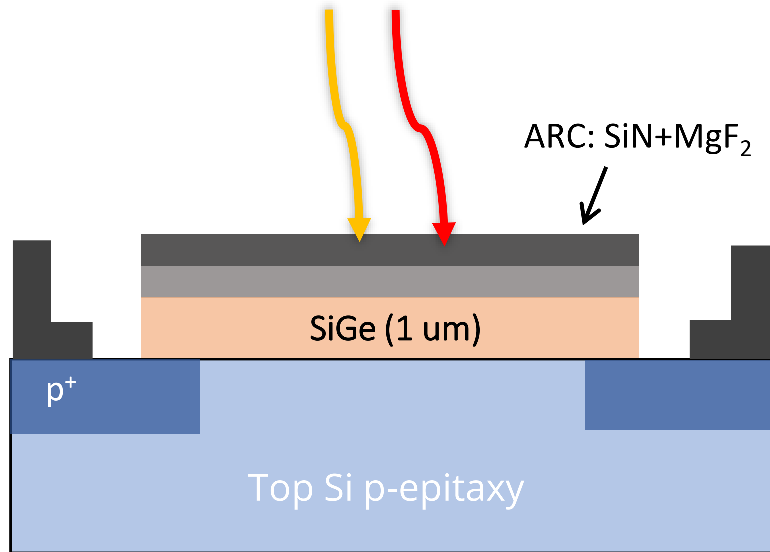


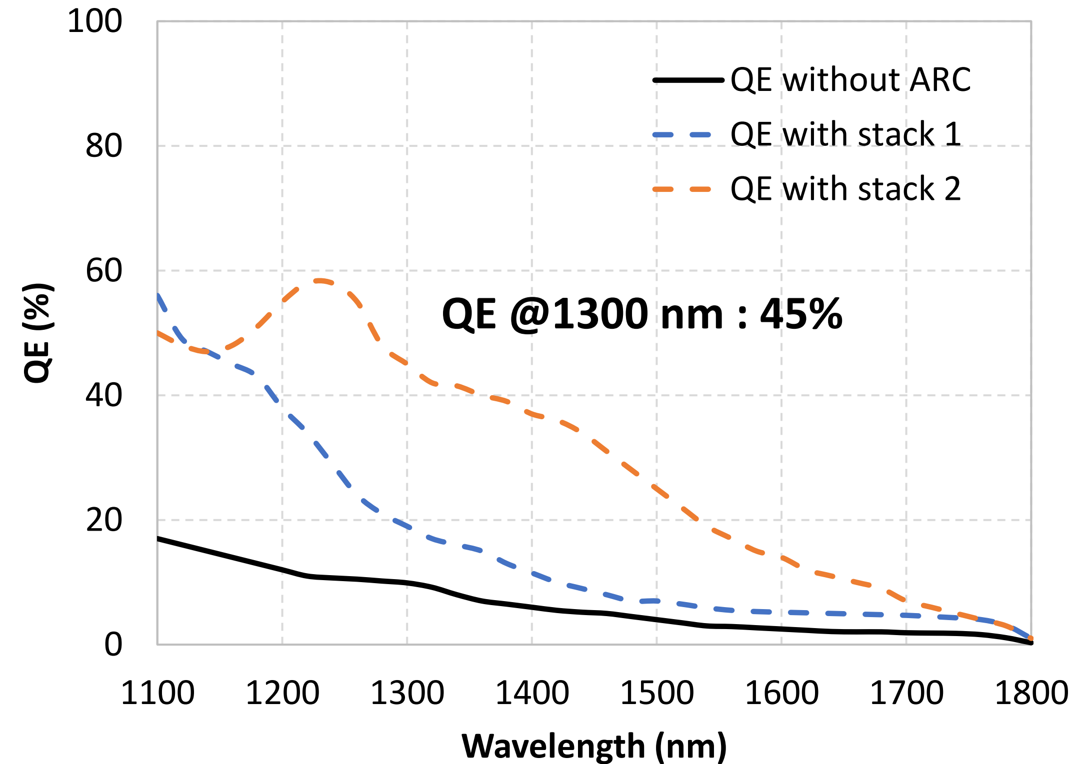
ARC: Anti-reflective Coating

Simulation of Optical Response in Ge-on-Si Photodiode

- With anti-reflective layer

Stack 2: SiN (100 nm)/MgF_2 (160 nm)





ARC: Anti-reflective Coating

Summary and Outlook

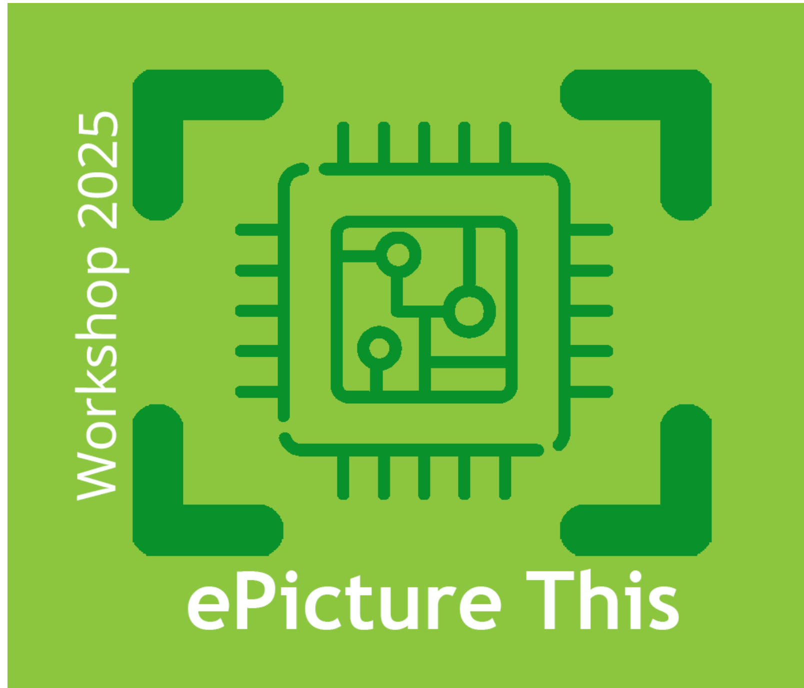
A low-temperature post-processing approach to enable broadband CMOS image sensors beyond the visible spectrum

CMOS compatible low-temperature crystalline growth of Ge on Si substrate

Low-temperature integration of Ge layer on Si photodiode

Preliminary results from optical characterization of Ge-on-Si photodiode

Ongoing work focuses on optimizing SWIR responsivity through process refinement and passivation techniques



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THANK YOU