CIS STACKING TECHNOLOGY
Past, Present, Future

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Harvest Imaging (B)

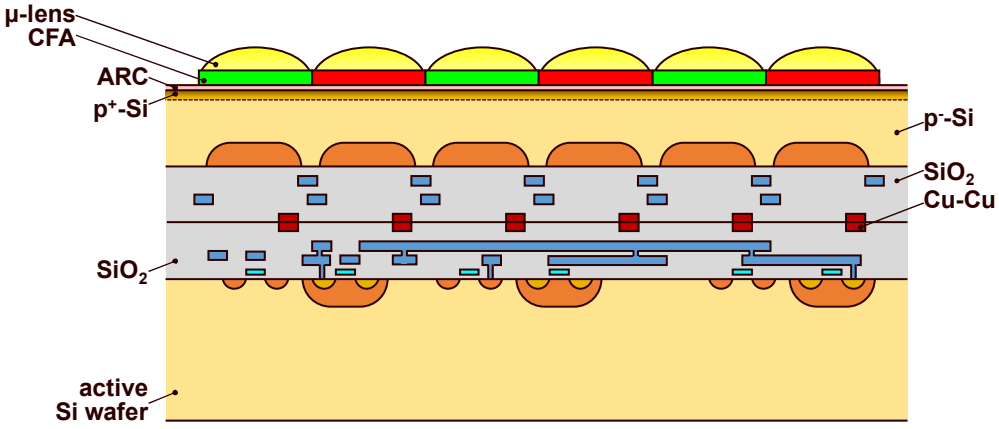
CIS Stacking Technology : Agenda

- Introduction to Stacking and Hybrid Bonding,
- Stacking to :
  - Improve CIS performance,
  - Extend the electronic volume of the pixel,
  - Add new features to CIS,
- Where to make the connection from the top layer to the bottom layer ?
- From W-to-W stacking to D-W stacking,
- Future Outlook,
- Further Reading.

CIS Stacking Technology : Definition

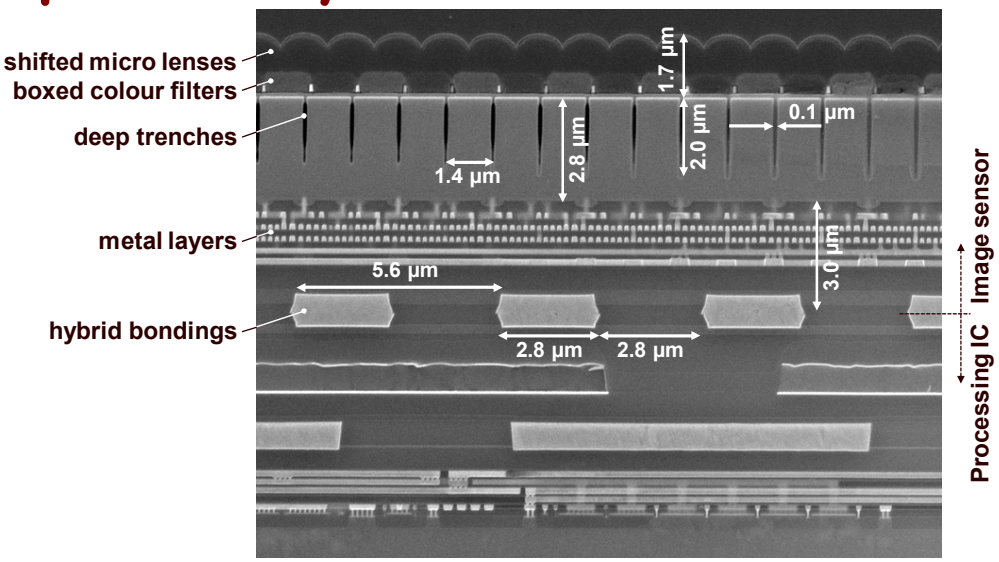
- Stacking means two or more electronic circuits placed on top each other and connected to each other,
- Stacking is already applied since a few decades in the memory world, first announcements can be found in publications of the '80s of previous century,
- By definition CIS stacking : a back-side illuminated imager is stacked on top of any other electronic circuit,
- Electric connections between the various stacked layers can be realized by :
  - Micro-bumps, used already for several decades in combination with BSI-CCDs for astronomy and space applications,
  - Through silicon vias (TSV),
  - Direct Cu-to-Cu contacts (Hybrid Bonding),
  - Combination of aforementioned methods.

Stacked Image Sensor : Hybrid Bonding (2)



- Deposition of colour filters and micro-lenses on the CIS backside.

Example : Galaxy S7 Sensor



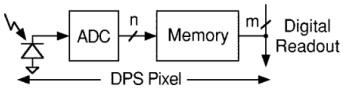
http://www.chipworks.com/about-chipworks/overview/blog/samsung-galaxy-s7-edge-teardown

Advantages of Hybrid Bonding

- Very compact structure :
  - Small(est) footprint (possible),
  - Low interconnect resistances and capacitances, fast and low-power interconnects,
- "Cheap" image sensor chip (n-MOS instead of CMOS),
- Optimized choice of fabrication technology for top and bottom layer,
- Not limited to visible RGB sensing, but also depth, temporal contrast, near-IR, …
- Not limited to W-to-W stacking, but also D-W stacking,

- Allows further improvement of CIS performance (noise, full-well, dynamic range, speed, …),
- Extends the "electronic volume" of the pixels (sub-micron pixels, wide dynamic range, global shutter, …),
- Allows pixel-level processing,
- Adds new features to the existing CIS devices.

Extension Pixel "Electronic Volume" (2)



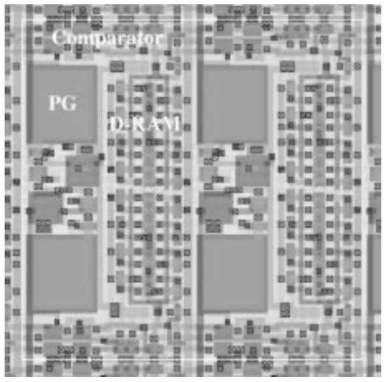
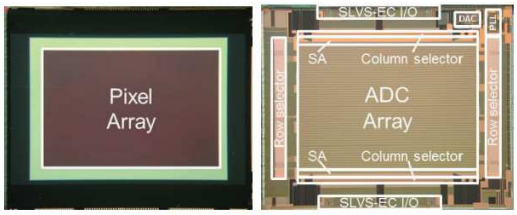


Fig. 5. DPS pixel layout (2 × 2 pixel block shown). Pixel size is 9.4 × 9.4 μm.

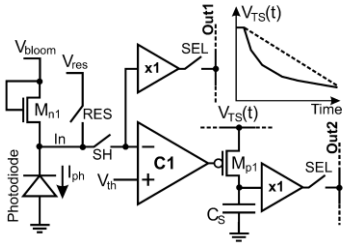
S. Kleinfelder, IEEE JSSC, 2001.

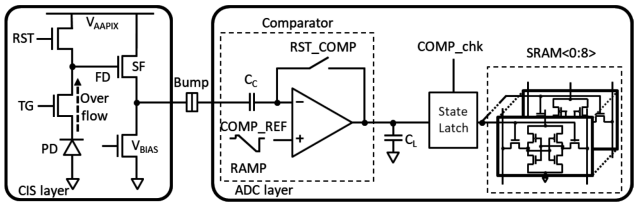


Item	Data
Process	Top: 90nm 1Poly-4Metal Bottom: 55nm 1Poly-7Metal
Supply voltage	2.9V/1.1V
Pixel size	4.8um(H) x 4.8um(V)
# of pixels	2360 (H) x 1728 (V)
Sensitivity	28400e- lx/s
Frame rate	Rolling shutter: 630fps FD Global shutter: 280fps
DNL/INL	±0.3LSB / <3.3LSB
Conversion gain	65uV/e-
Total random noise	4.2e⁻rms (Dark, A-gain 24dB)
Block random noise	0.40e⁻rms (Dark, A-gain 24dB)
Phase random noise	0.28e⁻rms (Dark, A-gain 24dB)

T. Takahashi, VLSI Symposium, 2017.

Extension Pixel "Electronic Volume" (3)





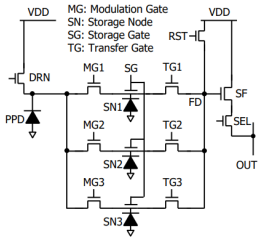
Technology	0.35µm, 3.3V CMOS (2P-4M)
Pixel pitch	15µmx15µm
Array size	140x140 pixel
Transistors per pixel	20
Die size	3.9x4.6mm^2
Power dissipation	200mW@30fps (including ADC) 30mW@30fps (analog part only)
Fill factor	20%
Sensor output	Two 10-b digital outputs
ADC DNL / INL	(+0.5, -0.4) / (+0.6, -0.5)
FPN (Out1,Out2)	<0.5%, <1.7%
PN (Out1,Out2)	0.13% rms
Dynamic range	120 dB (typical operation)
Dark current	90mV/sec @ T=30C

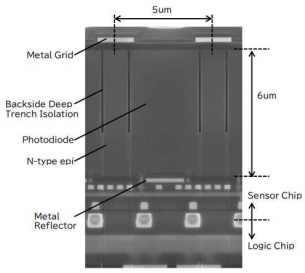
D. Stoppa, IEEE JSSC, 2007.

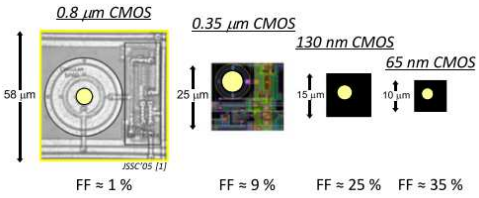
Specification	This work
Pixel architecture	DPS (pixel parallel)
Quantization scheme	2Q (PD-Time Stamp)
Pixel size [um]	4.0
In pixel Memory bit # (state bit #)	9b(1)
QE (@530nm) max [%]	90 (Mono)
Dynamic range [dB]	107
Conversion Gain [uV/e⁻]	150
Linear full well [ke⁻]	4/2000**
Noise floor [e⁻]	8.2
Dark FPN [e⁻]	63.9

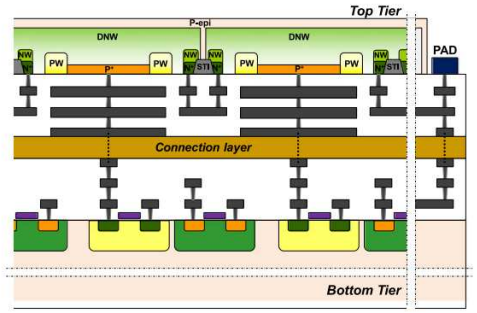
K. Mori, VLSI Symposium, 2021.

i-ToF and d-ToF









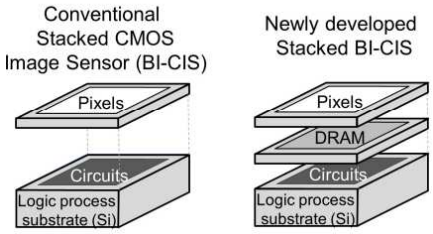
- **SPADs have a low fill-factor,**
- **Stacking can solve this problem !**

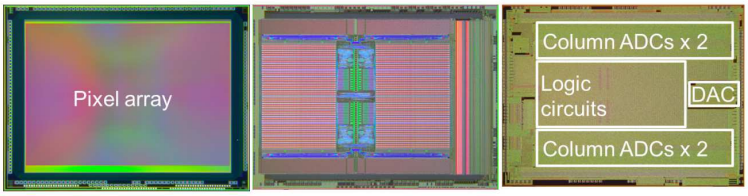
Y. Ota, ISSCC, 2022.

M. Tsutsui, IISW, 2021.

M.-J. Lee, IEEE QE, 2018.

Adding New Features





A micrograph of top layer

A micrograph of middle layer

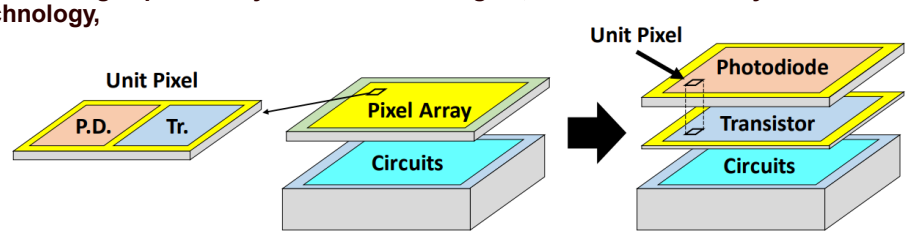
A micrograph of bottom layer

- **High-speed CIS are very often limited by the speed of the I/O,**
- **With a 3-layer stacked DRAM included, the I/O from CIS to DRAM can be very fast (in combination to a lower speed to the external periphery),**
- **Applications :**
  - **Slow motion for video,**
  - **Ultra-fast rolling shutter for digital photography (mechanical shutter no longer needed).**

T. Haruta, ISSCC, 2017.

Towards Pixel Splitting (1)

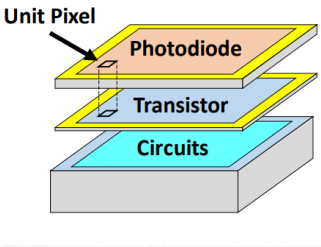
- Instead of having a connection in the charge domain and place the source-follower, reset and select on the logic layer, make a triple stacked device :
  - Top layer contains the photodiodes,
  - Middle layer contains the pixel transistors,
  - Bottom layer contains all logic circuits.
- Advantages : high full well, large fill factor, "large"-sized source follower (1/f and RTS noise),
- Disadvantage : potentially a low conversion gain, but this is solved by a more complex stacking technology,

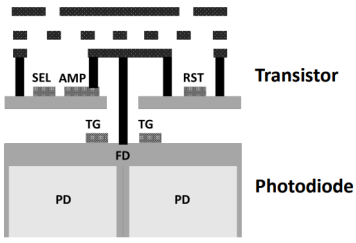


Conventional Structure 2-Layer Pixel

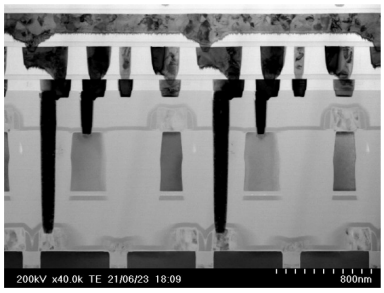
K. Nakazawa, IEDM, 2021.

Towards Pixel Splitting (2)





Unit Pixel



- 33 Mpixels, 0.7 µm pixel pitch,
- Double stacking (no stacking to circuits),
- Full Well Capacity : 2x,
- Low Random Noise (1/f noise, RTS).

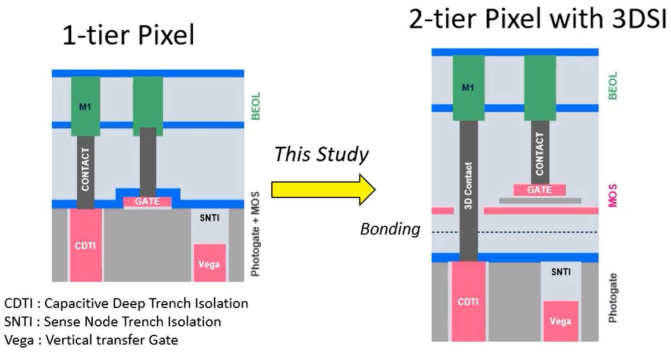
K. Nakazawa, IEDM, 2021.

Triple Stacking (1)

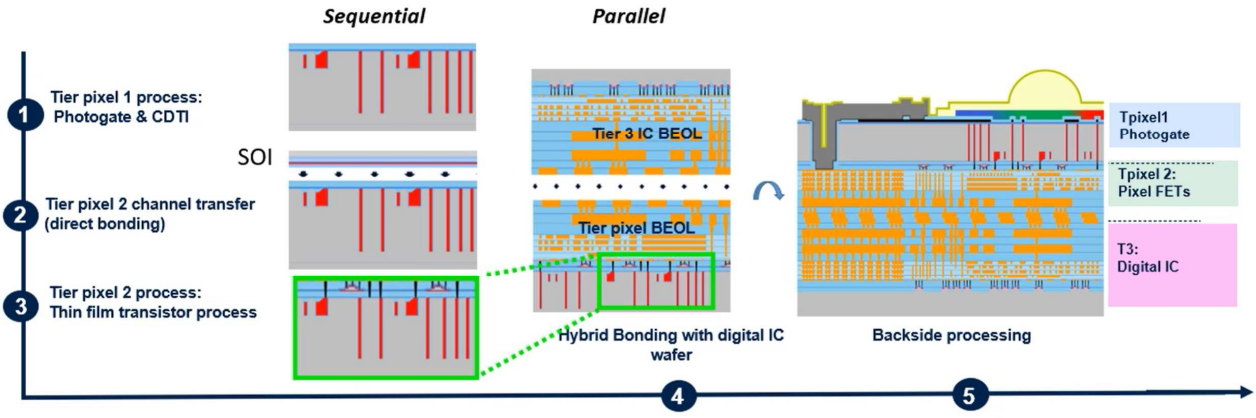
The imaging technology came to the point that the in-pixel transistors hamper further downsizing. Solution is to use multiple stacking layers :

- **The first layer contains the photo-conversion part :**
  - **Optimized fill factor,**
  - **Optimized full well,**
- **The second layer contains the in-pixel transistors :**
  - **Optimized noise (1/f and thermal noise),**

(Sony presented this solution at IEDM 2021 in a two-layer technology).

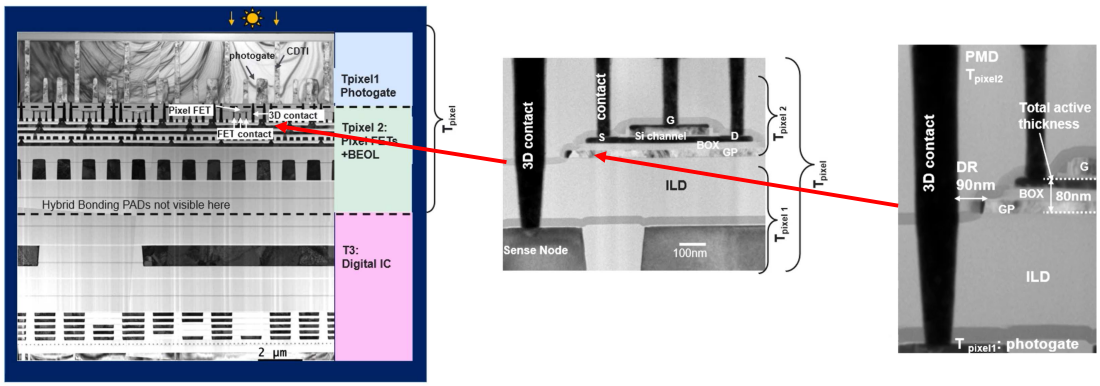


Triple Stacking (2)

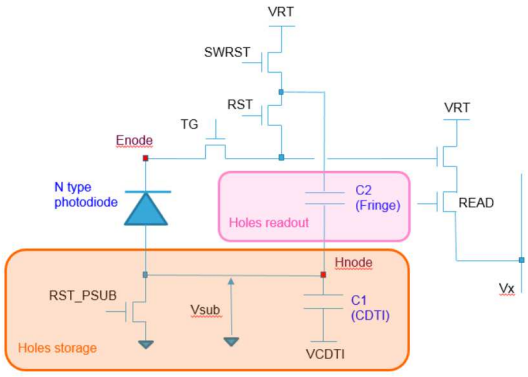


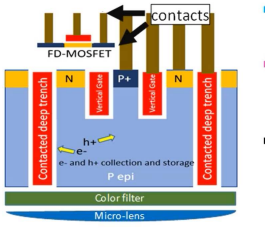
Triple Stacking (3)

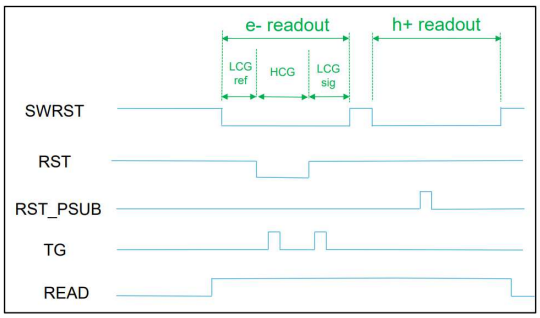
3-Tier BSI CIS stacking



Pixel Structure : e⁻ and h⁺ Collection



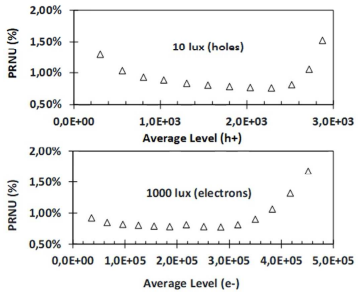




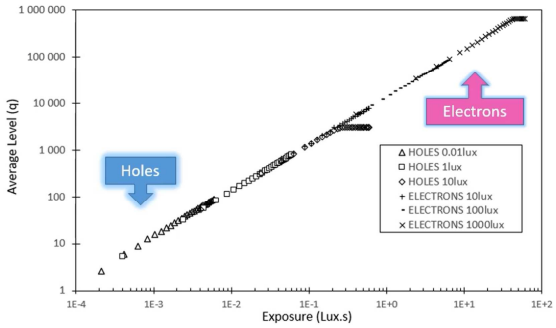
To make use of electrons and holes, the quantum efficiency for both NEEDS TO BE EQUAL !!! This is only possible if the collection volume is fully isolated.

Performance (1)

Photo-Response Non-Uniformity (PRNU)



Pixel linearity for holes and e- versus exposure



Performance (2)

Single Exposure Performance Landscape

Pixel Summary

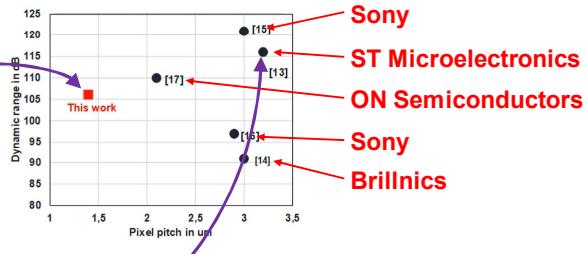
High Conversion gain holes	106 µV/h+
Conversion gain electrons	0.625 µV/e-
Usable Full Well holes	2,500 h+
Usable Full Well electrons	400,000 e-
High Frequency PRNU holes	0.80 %
High Frequency PRNU electrons	0.80 %
Idark holes	4 h+/s
Idark electrons	20,000 e-/s
Temporal Noise in High CG Mode	2 h+
Dynamic range (FPN not included)	106 dB

1.4 µm

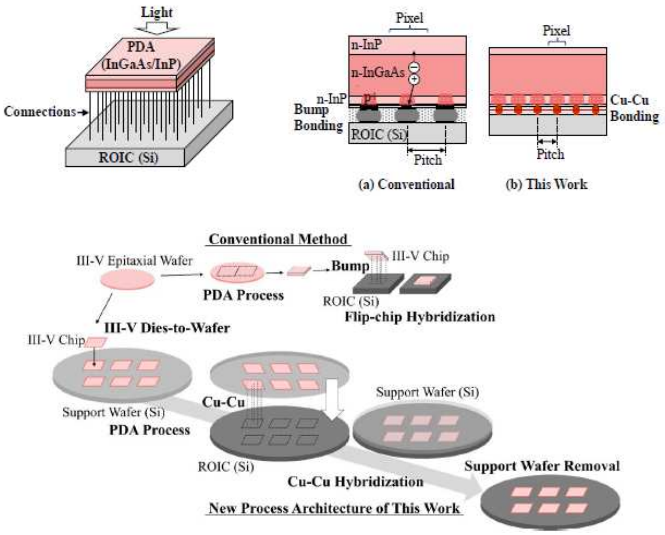
Performance	Unit	Value
High Conversion gain electrons	µV/e−	163
Low Conversion gain electrons	µV/e−	29.6
Conversion gain holes	µV/h+	1.33
Usable Full Well electrons	e−	33,000
Usable Full Well holes	h+	750,000
High Frequency PRNU electrons		0.55%
High Frequency PRNU holes		0.41%
Idark electrons	e−/s	45
Idark holes	h+/s	2300
Noise Floor in High CG Mode	e−	1.2
Dynamic range	dB	116
Green QE peak		73%

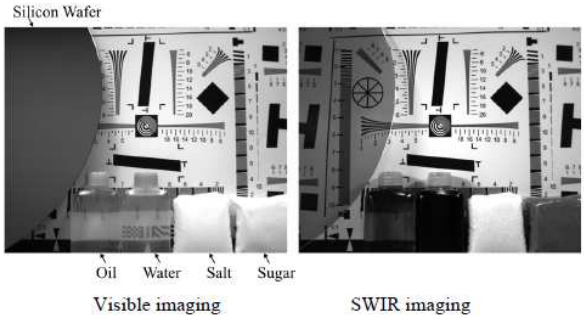
3.4 µm

PRNU: pixel response non-uniformity; QE: quantum efficiency.



Die-to-Wafer Stacking (1)

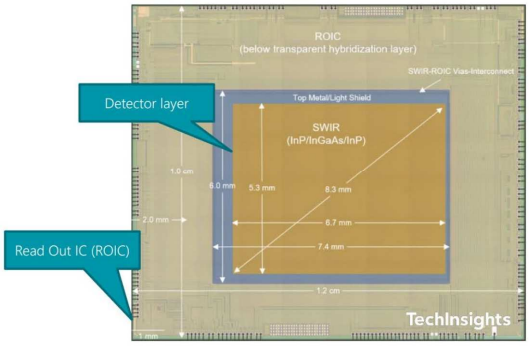


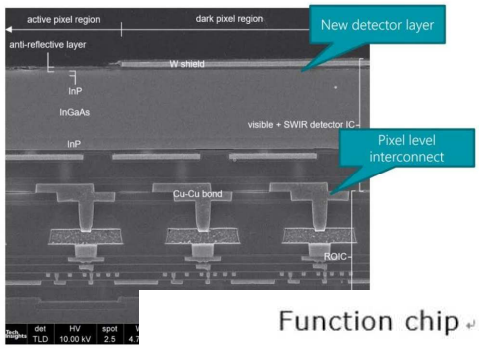


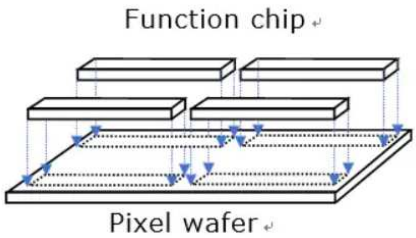
- 1.3 Mpixels, 5.0 µm pixel pitch,
- 1550 nm SWIR,
- 40 °C.

S. Manda, IEDM 2019.

Die-to-Wafer Stacking (2)







- The stacked die no longer has to match the form factor of the "carrier",
- More than one die can be stacked to a single "carrier" (µ-bumps),
- The stacked die can be the imager or can be the digital circuit.

TechInsights, Reverse Eng. Report IMX990, 2021

Y. Oike, VLSI Symp., 2016

Future Outlook (1)

- More triple-layered structures are on their way in which two layers will be used for the pixels :
  - Further increase the dynamic range of small-pixel devices,
  - Create global shutter functionality in the voltage domain (see announcement this week by OV),
- iToF pixels will become as small as today's global shutter pixels, performance improvement of dToF based on SPADs, e.g. PDE, speed and power (towards 1Tops/W),
- Tomorrow's SPAD technology will be based on today's mobile imaging technology,
- SWIR applications require the combination of "foreign" materials and a silicon ROIC, stacking is ideally suited for this technology, D-2-W stacking opens new horizons,
- Stacking makes pixel-level processing possible and will pave the path to intra-pixel processing,
- Stacking will allow that the image sensor will become the first layer of a neural network,

Future Outlook (2)

- New CIS developments will focus on advanced packaging of which stacking will be part of,
- Dedicated equipment is becoming more widely available, also to the pixel-level imaging world : W-2-W and D-2-W machines,
- What about the heat dissipated "underneath" the pixels ? What about yield (x·y) ? Should the stacked layers have the same physical size ?
- Can the (consumer, mobile) imaging market make enough money to support the continuous need for more advanced technologies ?
- Stacking is enlarging the technology gap between the most advanced imaging fabs and the ones that use a "standard" technology,
- What about low-volume applications ? What about access to stacking for research activities ?

(A MUST !!!) Further Reading

2766 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 69, NO. 6, JUNE 2022

A Review of 3-Dimensional Wafer Level Stacked Backside Illuminated CMOS Image Sensor Process Technologies

Shou-Gwo Wuu, *Member, IEEE*, Hsin-Li Chen, *Member, IEEE*, Ho-Ching Chien, Paul Enquist, *Senior Member, IEEE*, R. Michael Guidash, *Member, IEEE*, and John McCarten

(Invited Paper)

~~Rockin' and Stackin'~~

Keep on ~~Rockin'~~ in a FREE WORLD !

Thank You.